A CAHNERS PUBLICATION INTERNATIONAL EDITION MARCH 29, 1990

EDN®

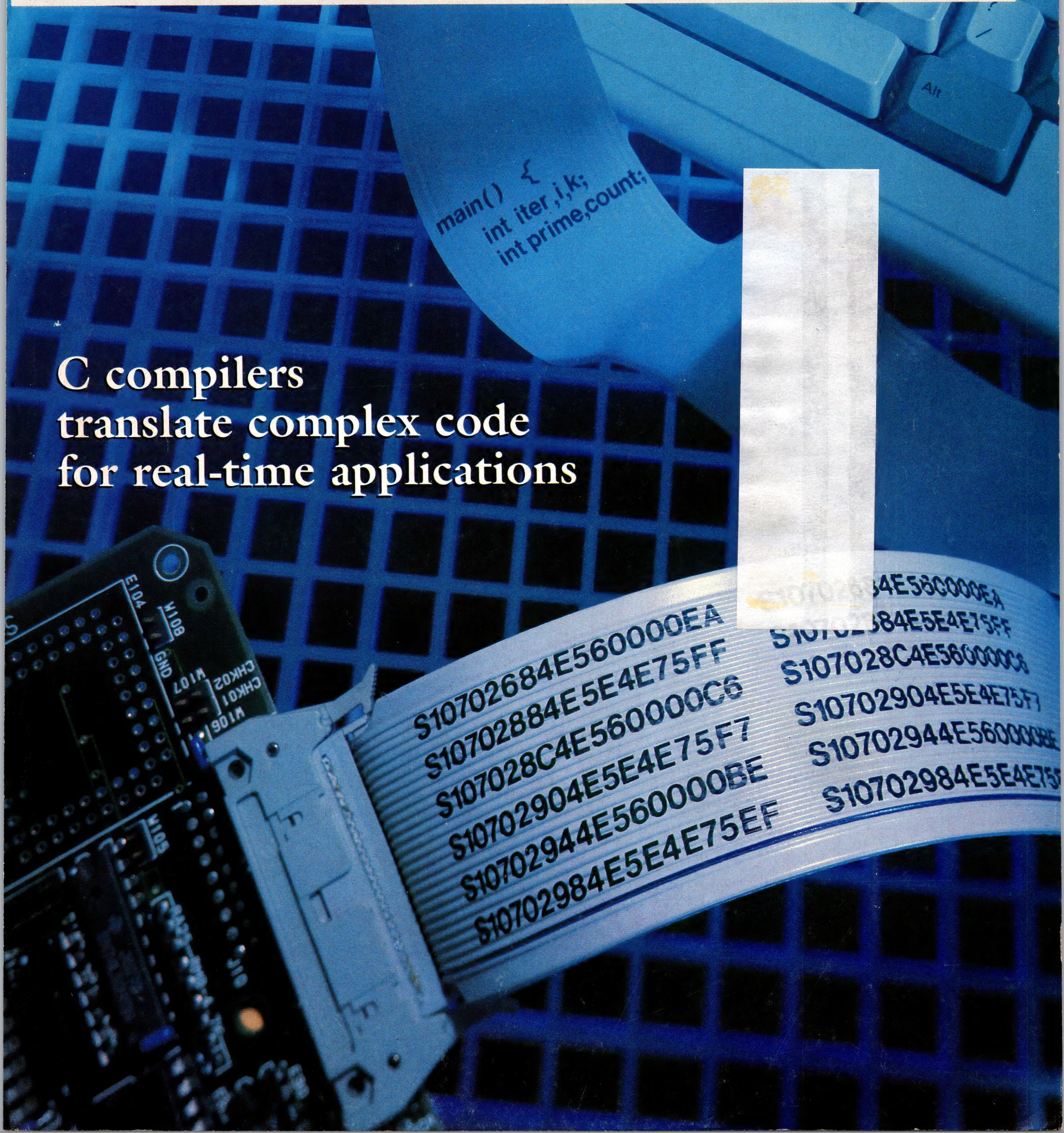
SPECIAL ISSUE: Software

Improving code for vector/parallel computers

Optimizing C compilers for single-chip μPs—Pt 1

EDN's All-Star PC—Pt 2

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



C compilers translate complex code for real-time applications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ABSORPTIVE...REFLECTIVE

dc to 4.6GHz from $32.95 (10-24)

Tough enough to pass stringent MIL-STD-883 vibration, shock, thermal shock, fine and gross leak tests...useable to 6GHz...smaller than most RF switches...Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

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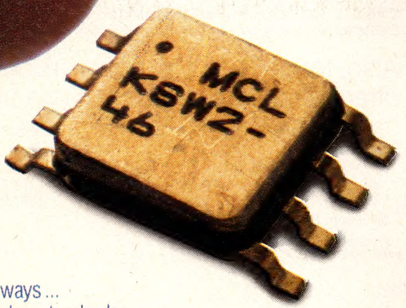
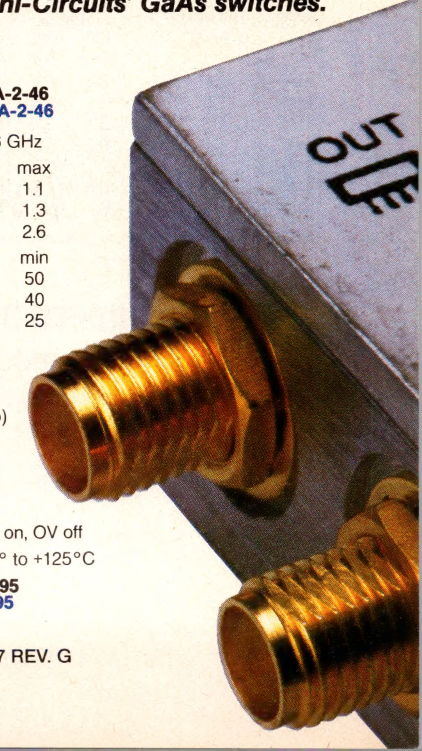


SPECIFICATIONS

		KSW-2-46		KSWA-2-46	
Pin Model		**KSW-2-46**		**KSWA-2-46**	
Connector Version		**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE		dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)		typ	max	typ	max
dc-200MHz		0.9	1.1	0.8	1.1
200-1000MHz		1.0	1.3	0.9	1.3
1-4.6GHz		1.3	1.7	1.5	2.6
ISOLATION (dB)		typ	min	typ	min
dc-200MHz		60	50	60	50
200-1000MHz		45	40	50	40
1-4.6GHz		30	23	30	25
VSWR (typ)	ON	1.3:1		1.3	
	OFF	—		1.4	
SW. SPEED (nsec) rise or fall time		2(typ)		3(typ)	
MAX RF INPUT (bBm)					
up to 500MHz		+17		+17	
above 500MHz		+27		+27	
CONTROL VOLT.		-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.		-55° to +125°C		-55° to +125°C	
PRICE (10-24)		**$32.95** **$69.95**		**$48.95** **$79.95**	



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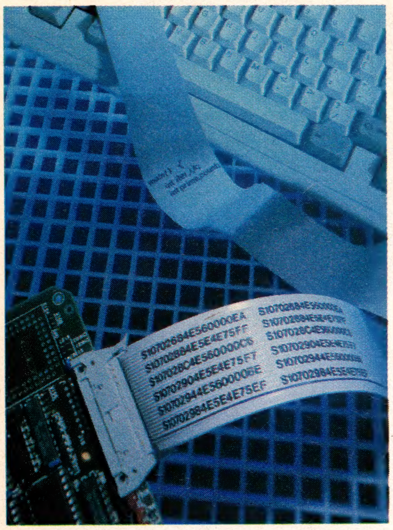
CIRCLE NO. 3

EDN Magazine Edition®

Volume 35, Number 7

March 29, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Advances in optimization techniques allow C compilers to produce code that's fast enough for real-time systems. See the Special Report on pg 96. (Photo courtesy Intermetrics Inc)*

SOFTWARE SPECIAL ISSUE

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

EDN®(ISSN 0012-7515) is published 49 times a year (biweekly with 2 additional issues a month, except for February, which has 3 additional issues and July and December which have 1 additional issue) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Senior Vice President/General Manager, Boston Division; Jerry D Neth, Senior Vice President/Publishing Operations; J J Walsh, Senior Vice President/Finance; Thomas J Dellamaria, Senior Vice President/Production and Manufacturing; Ralph Knupp, Vice President/Human Resources. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. POSTMASTER: Send address corrections to EDN® at the Denver address. EDN®copyright 1990 by Reed Publishing USA; Ronald G Segel, Chairman and Chief Executive Officer; Robert L Krakoff, President and Chief Operating Officer; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $105/year; Canada/Mexico, $125/year; Europe air mail, $150/year; all other nations, $150/year for surface mail and $230/year for air mail. Single copies are available for $10. Please address all subscription mail to Eric Schmierer, 44 Cook Street, Denver, CO 80206-5800.

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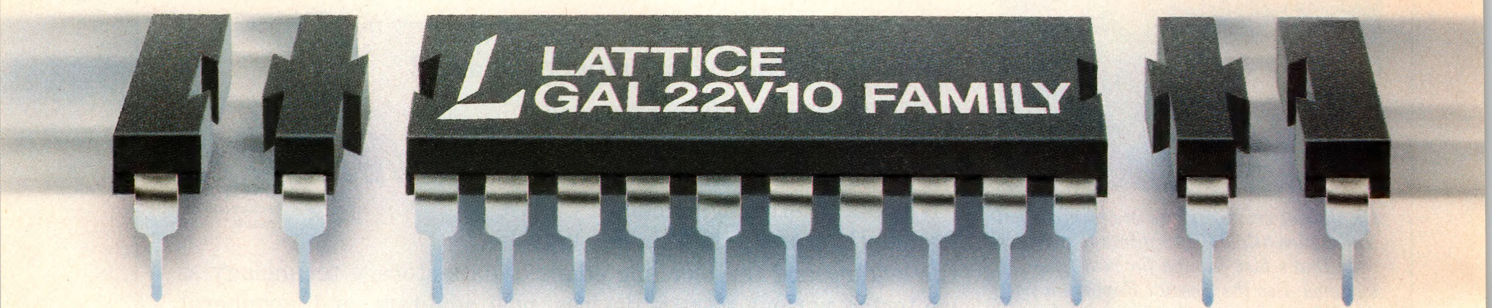

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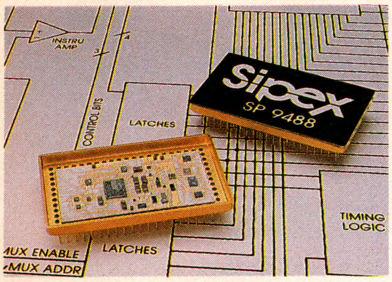
Continued from page 5

EDN Magazine Edition

March 29, 1990



Reap the benefits of using highly integrated ICs, *such as multichannel sampling ADCs, by deciding what combination of features and performance is most economical for your design (pg 59).*

TECHNOLOGY UPDATE

EDITORS' CHOICE

PRODUCT UPDATES

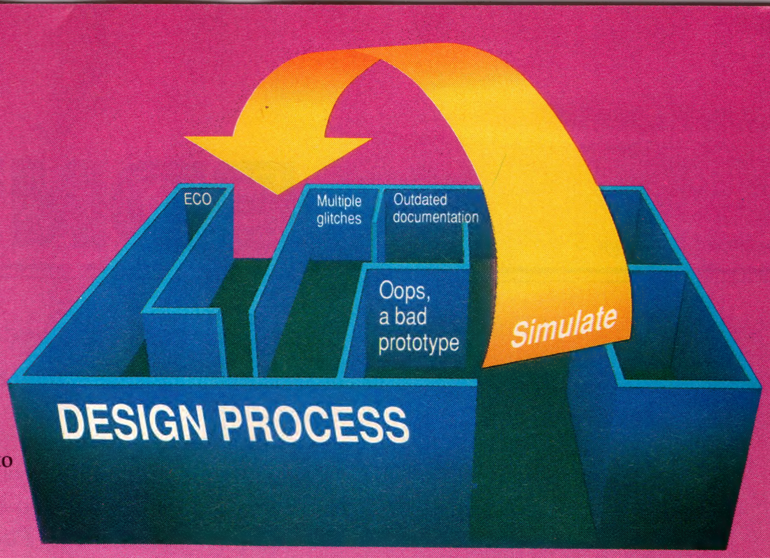
DESIGN IDEAS

Continued on page 9

Cahners Publishing Company, A Division of Reed Publishing USA ☐ Specialized Business Magazines for Building & Construction ☐ Manufacturing ☐ Foodservice & Lodging ☐ Electronics & Computers ☐ Interior Design ☐ Printing ☐ Publishing ☐ Industrial Research & Technology ☐ Health Care ☐ and Entertainment. Specialized Consumer Magazines: ☐ American Baby ☐ and Modern Bride.

OrCAD Answers Your Questions About

Logic Simulation



Q: Why simulate?

A: To save time.

The ideal development cycle is schematic to prototype to production. Simulation dramatically decreases the dreaded loop of schematic to prototype to schematic to prototype to schematic to...

A: To save money.

If your design goes through several iterations, is the documentation still accurate? Suddenly your time and budget are being spent on laying in patches, not producing.

A: To make you look good.

Your schematic is supposed to be the best answer to someone else's design problem. Think of how great you'll look when you present a solution with no glitches, timing violations or other problems.

Verification of your design doesn't have to be handled at the prototype stage (or worse yet, the production stage).

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You need a digital simulator that helps you find timing violations and design anomalies before you spend time and money on prototypes. The result: fewer iterations, a shorter design cycle, a more reliable product and getting the project right.

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A: OrCAD/VST enables you to interactively verify your design as it develops. A netlist from OrCAD's powerful Schematic Design Tools is all that's required to get started.

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EDITORIAL

Don't mourn the demise of US Memories, a consortium that was to produce DRAM chips in the US. The companies that turned down the opportunity to join the group—or that were opposed to the consortium—knew what they were doing.

NEW PRODUCTS

PROFESSIONAL ISSUES

This article is the first in an occasional series exploring aspects of modern business.—*Jay Fraser, Associate Editor*

DEPARTMENTS

"WE DEPEND ON **EDN'S MAGAZINE** AND **NEWS EDITIONS** TO DELIVER THE SPECIFICS ON MAXIM PRODUCTS TO POTENTIAL CUSTOMERS."

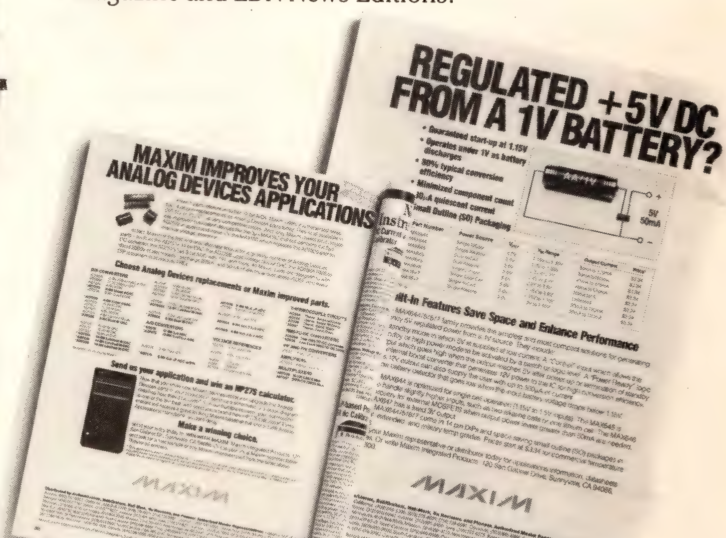
Mike Dikas
Director of Communications
Maxim Integrated Products

Maxim Integrated Products is one of today's fastest growing international suppliers of quality analog ICs. In the past five years they have introduced more than two hundred proprietary and improved second source devices.

Director of Communications, Mike Dikas has piloted Maxim's advertising program since its inception. "EDN's magazine and news editions have played a significant role in introducing many of our new products. In the past two years, over 25,000 EDN Magazine and News Edition readers have responded to Maxim ads, product releases and articles," says Mike. "Our ads consistently fall in the top 10% in reader response in both editions of EDN. What's even more amazing is that we typically get less than 5% duplication of responses to the same ad in both the Magazine and News Editions."

What's that mean for Maxim? "Since both editions deliver the same circulation, it's apparent to us that the same engineers read both the Magazine and News Editions for different reasons. Given Maxim's charter of product proliferation, EDN's in-depth coverage of technical issues and timely coverage of new products are both of the utmost importance to Maxim."

Mike Dikas believes in the complementary roles of EDN Magazine and EDN News Editions.



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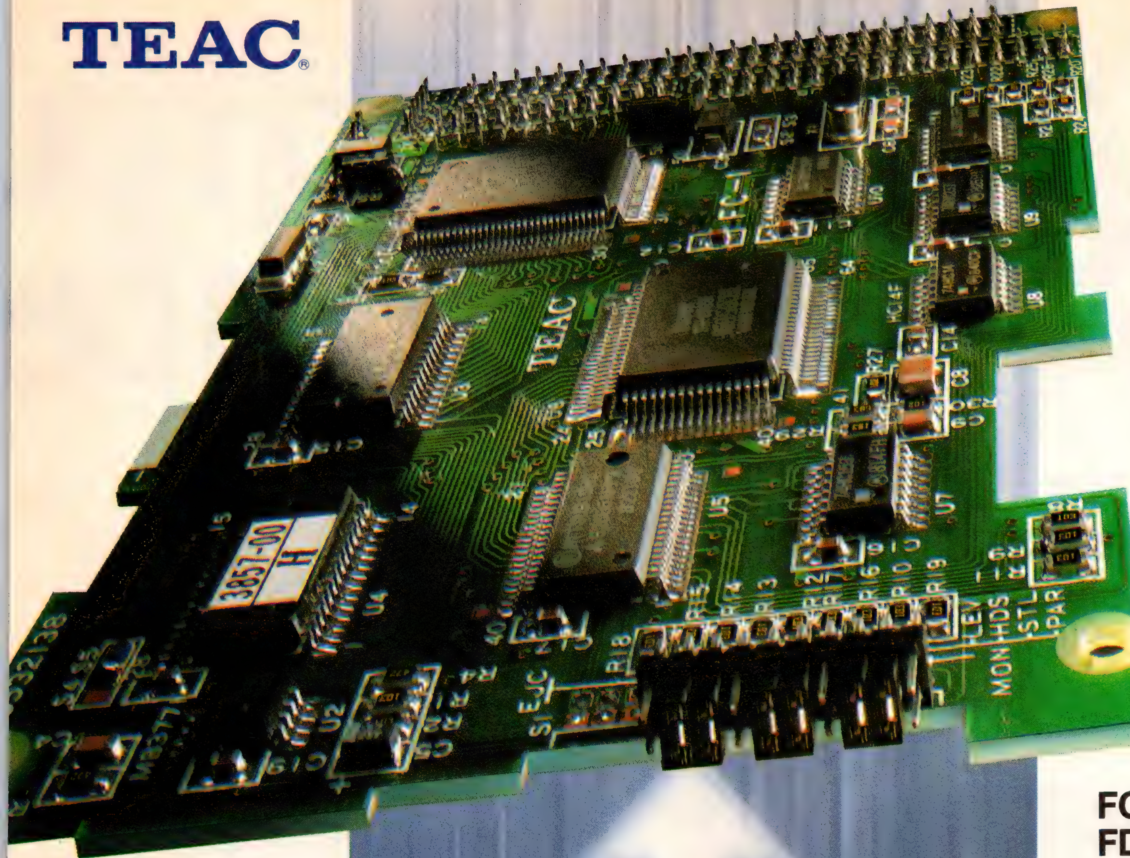

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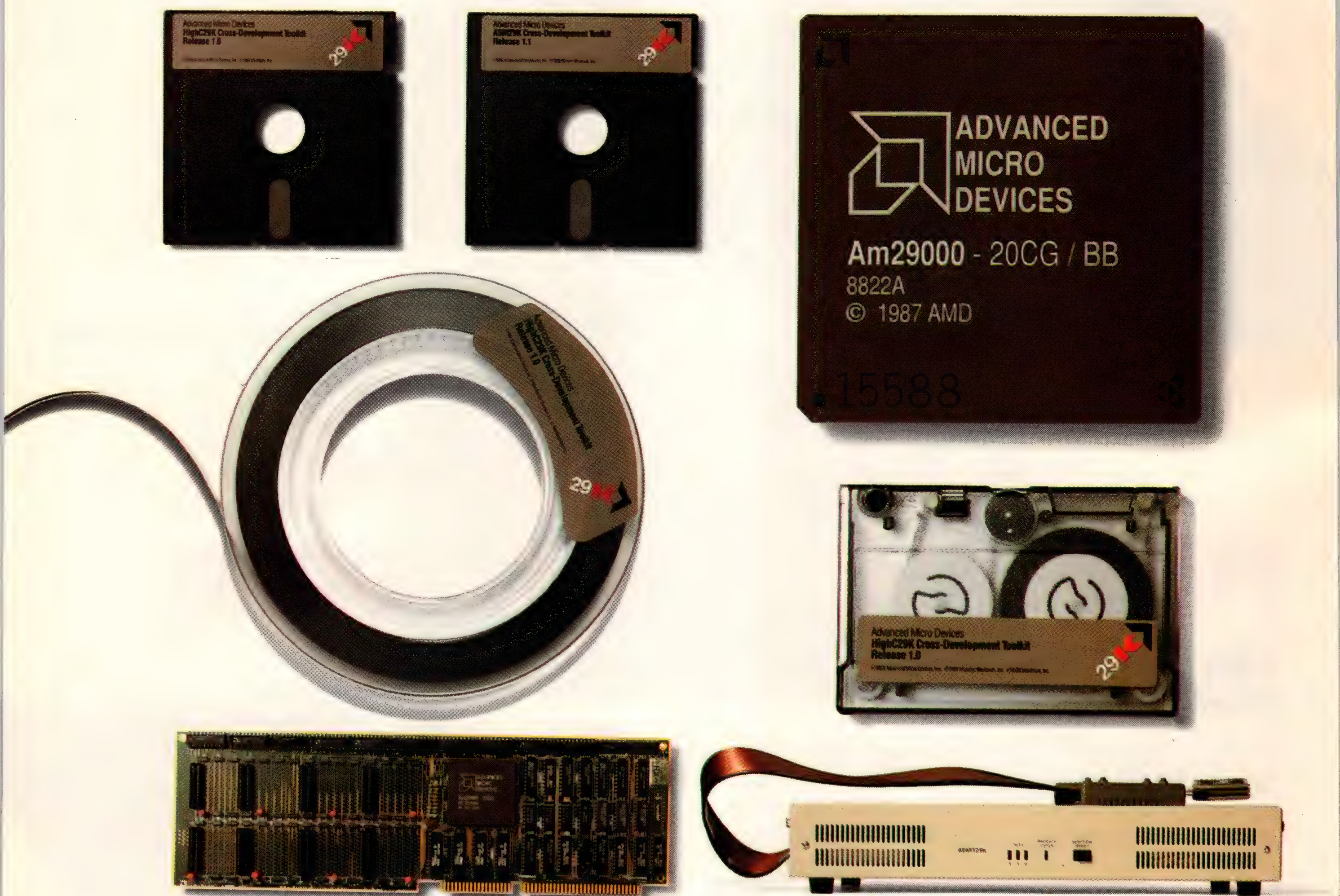

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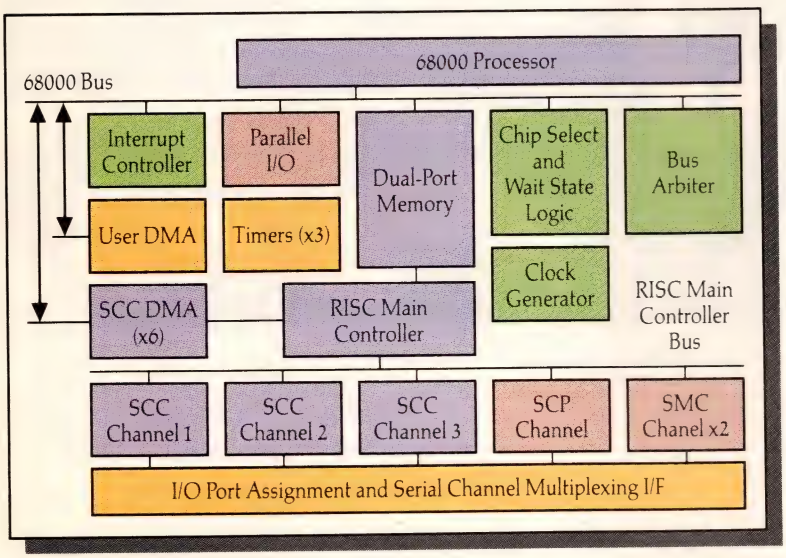
To save you even more money (and a bit of board space), the 68302 is the most highly integrated communications controller around. In addition to its mighty processors, it comes with a system integration module that's loaded with system glue logic (see diagram for details) you'd otherwise have to provide yourself.



COMMUNICATE TOLL FREE.

So whether you're designing for ISDN or any other form of communication, you simply can't do any better than the 68302.

For more information on the 68302, the third-party support behind it, and our 68302 Application Development Systems Evaluation Board, call 1-800-441-2447. Or contact the Motorola Semiconductor sales office nearest you.

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	KM6465L	16K x 4	25/35/45ns	SDIP
	KM6865	8K x 8	35/45/55ns	SDIP
	KM6865L	8K x 8	35/45/55ns	SDIP
256K	KM61257	256K x 1	25/35/45ns	SDIP/SOJ
	KM61257L	256K x 1	25/35/45ns	SDIP/SOJ
	KM64257	64K x 4	25/35/45ns	SDIP/SOJ
	KM64257L	64K x 4	25/35/45ns	SDIP/SOJ
	KM68257P	32K x 8	35/45/55ns	DIP
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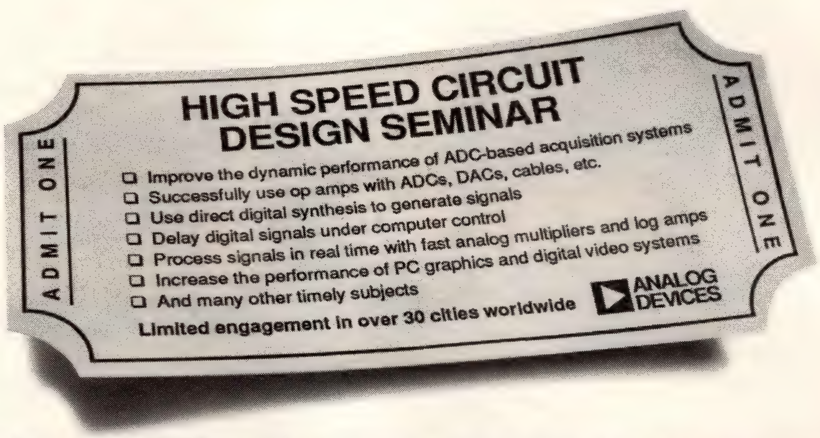

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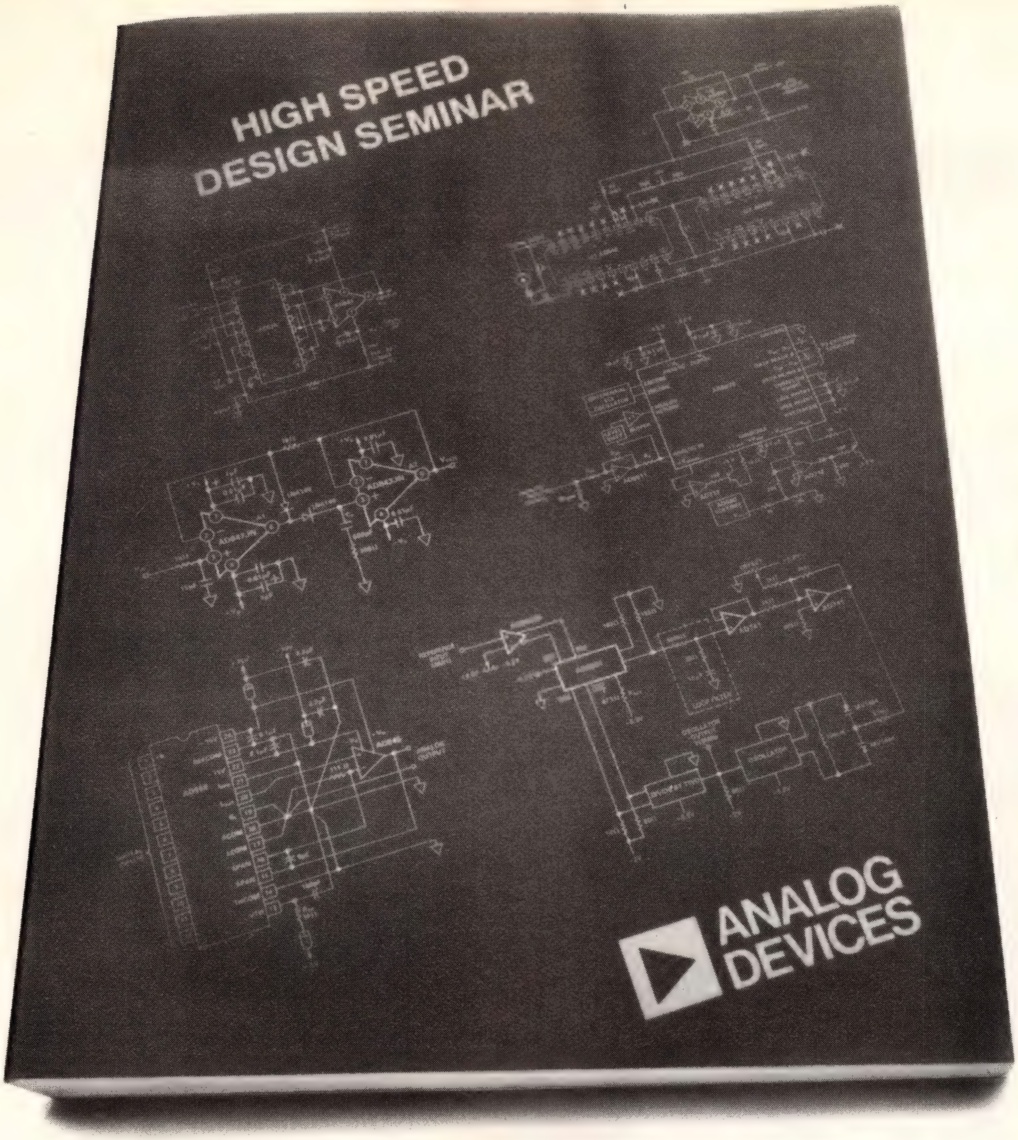

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NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

MACINTOSH GETS NEW CPU AND GRAPHICS

Apple Computer (Cupertino, CA, (408) 996-1010) recently introduced a 40-MHz 68030-based Macintosh and three color graphics boards. The Macintosh IIfx makes use of distributed intelligence. Typical configurations will include a 1.4M-byte floppy-disk drive and an 80M- to 160M-byte hard-disk drive, and will cost $10,000 to $12,000. You can also purchase the CPU board as an upgrade to your Macintosh II.

The graphics boards all offer monochrome and color capabilities and can drive all Macintosh monitors. The Picasso 4/8 has monochrome resolutions as high as 1152×870 pixels with 16 gray levels and 640×480 pixels with 256 colors. The Picasso 8/24 offers 256 gray levels and 16.7 million colors at the same maximum resolutions. The boards cost approximately $700 and $1000, respectively, and you can upgrade the 4/8 to 8/24 capabilities. The Monet board includes display capabilities comparable to those of the Picasso 8/24 and performs under the control of a 30-MHz AMD 29000 RISC µP.—Maury Wright

SCHEMATIC-DESIGN TOOL LETS YOU USE PCs

CF3000M, an IBM PC-based version of Phase Three Logic Inc's (Beaverton, OR, (503) 645-0313) CapFast schematic-design package, can interchange symbol libraries and schematics with Mentor Graphics' design systems. This feature lets you create schematics on low-cost PCs instead of on more expensive engineering workstations. The package follows the EDIF (Electronic Design Interchange Format) 2.0.0 specification to perform schematic-, symbol-, and net-list-level translation. Thus, symbols and schematics appear identical on both design systems. The package requires an 80386 µP-based IBM PC and costs $15,000 for a 10-user license.—Steven H Leibson

MODULAR SUPPLIES ATTAIN 3.5W/in.^{3} POWER DENSITY

The Omega series of modular power supplies from Coutant Lambda (Ilfracombe, UK, FAX (271) 864894) includes six models, each of which has as many as four isolated outputs in combinations of 5, 12, and 24V. The models drive 400W at 50°C with 80% efficiency from a 2.5×5.0×11.0-in. fan-cooled enclosure. You can adjust the nominal output levels from −40 to +20% to 1% resolution and preset the supply for line operation at 85 to 265V and 47 to 63 Hz. You can configure the supplies such that the outputs are available from terminals on the side or end of the units. Model MML400E2 supplies 5V at 60A and 5, 12, or 24V at 12A and costs £400 (50). —Brian Kerridge

CMOS MATH COPROCESSOR CUTS POWER, RUNS FASTER

A CMOS equivalent of the 80387SX math coprocessor executes math instructions at least five times faster and consumes less power. The Cyrix (Richardson, TX, (214) 234-8388) CX-83S87 is pin-for-pin and instruction-set compatible with Intel's (Santa Clara, CA, (408) 987-8080) 80387SX. The chip consumes 5 mA in standby and 40 mA when processing. The 16-MHz version costs $569; the 20-MHz version costs $640.—Charles H Small

NEWS BREAKS

MACINTOSH LEAVES APPLE CLOISTER, ENTERS REAL WORLD

Apple Computer's (Cupertino, CA, (408) 996-1010) new version of A/UX will please designers who want to use the Mac as a CAE tool. Version 2.0 of the Macintosh Unix operating system is compatible with X-Windows, traditional character-based Unix, and "32-bit clean" Macintosh applications. Therefore, users will have access to industry-standard Motif-based and Open Look X-Windows-based applications. The operating system manages both Unix and Macintosh file systems, and standard Macintosh applications suffer little degradation when run under A/UX. Version 2.0 of A/UX is based on Unix System V Release 2 and includes Berkeley extensions, TCP/IP (Transmission Control Protocol/Internet Protocol), and NFS (Network File System).
—Maury Wright

CELL LIBRARY OPTIMIZES ANALOG PERFORMANCE

Harris Semiconductor's (Melbourne, FL, (305) 724-7800) BiCMOS library for cell-based custom design suits applications that require high performance from the analog portion of a circuit. The BiCMOS process combines 3-μm CMOS with isolated, 300-MHz, vertical pnp bipolar transistors. MOSFET structures can implement voltage levels of 16V at 0.5A. The HBC2500 library contains 60 analog and 60 digital cells. A typical design could include as many as 50 analog cells and 1000 logic gates. The analog cells include a variety of op amps and comparators with both bipolar and MOSFET inputs. Inclusion of both input types lets you choose between high-performance (±2-mV offset) and medium-performance (±20-mV offset) analog cells. Other analog cells include trimmable bandgap references, an 8-bit current-steered D/A converter, oscillators, 0.5A power drivers with current and temperature sensing, and level shifters. The company plans to announce a semicustom version of the library this summer.—Anne Watson Swager

8-PIN CHIP CONVERTS 240V AC TO 5 TO 24V DC FOR $2.93

You can directly convert 240V ac to 5 to 24V dc with the HV-2405E, a plastic, 8-pin IC from Harris Semiconductor (Melbourne, FL, (407) 724-7044). With the addition of four capacitors and a resistor, the device functions as a nonisolated dc power supply capable of delivering more than 50 mA. The IC incorporates short-circuit protection and costs $2.93 (1000).—Steven H Leibson

WORKSTATIONS OFFER PERFORMANCE BUT LITTLE SOFTWARE

A new family of workstations from IBM (White Plains, NY, (203) 352-7611) could cut the computer behemoth a slice of the workstation pie. The workstations feature a superscalar architecture. The low-end RS/6000-320 produces a SPEC (Standard Performance Evaluation Corp) rating almost three times higher than a SPARCstation 1 and more than double that of the DECstation 3100 and HP 9000-834. The midrange and high-end workstations also offer extremely competitive performance. Perhaps most surprising, however, is the pricing of the workstations; prices for the entry-level RS/6000-320 start at under $13,000. While these machines clearly surpass the brain-dead IBM RT PC, the CAE-applications list for them is mighty short. Valid (San Jose, CA, (408) 432-9400) and Viewlogic Systems (Marlborough, MA, (508) 480-0881) are the CAE shining stars that could act as a beacon for other CAE developers and users.—Michael C Markowitz

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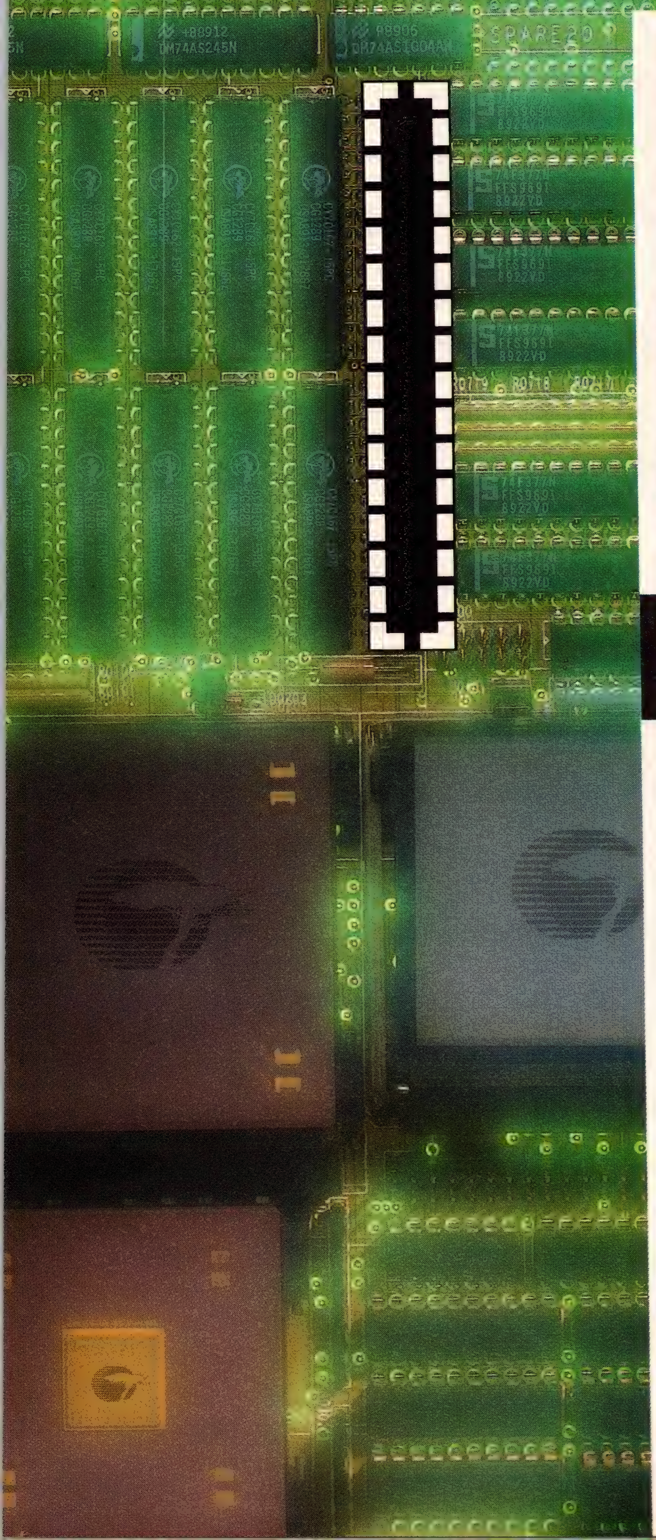

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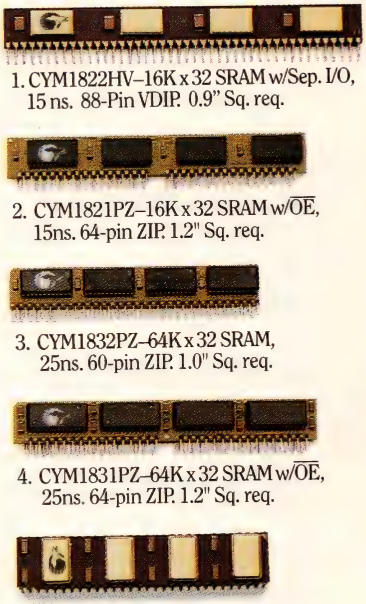

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RAD-HARD ICs CARRY OFF-THE-SHELF PRICE TAG

The United Technologies Microelectronics Center (Colorado Springs, CO, (719) 594-8259) now offers most of its standard and ASIC military ICs with guaranteed tactical or strategic radiation-hardness levels at standard-level prices. Designers of military equipment usually pay a fee in addition to the part cost to qualify any IC used in a military system that must meet radiation-hardness requirements. The company provides parts that meet the MIL-M-38510 standard for tactical applications—levels M (3×10^3 rads (Si)) and D (1×10^4 rads (Si))—or strategic applications—levels R (1×10^5 rads (Si)) and H (1×10^6 rads (Si)). These parts include radiation-hardness guarantees on the data sheet. For parts meeting radiation-hardness levels M and D, prices are comparable to the company's nonradiation-hard parts. Prices are higher for parts meeting the strategic radiation-hardness levels.—Steven H Leibson

VGA GRAPHICS BOARD DRIVES FLAT-PANEL DISPLAYS AND CRTs

The Display Master VGA graphics controller can drive EL (electroluminescent) and ac-plasma flat-panel displays, LCDs (including those with 12-bits of color), and color and monochrome CRTs. Yamaha (San Jose, CA, (408) 437-3133) includes with the board an extensive manual, which details DIP-switch settings for more than 50 popular flat-panel displays. Automatic initialization ensures that the card is set up properly before power is applied to a display. The card is compatible with CGA, EGA, VGA, and Hercules graphics standards and with IBM PCs. It costs $395 and is available 60 days ARO.—Maury Wright

SPICE SIMULATOR TRAINING CLASSES FOR ALL LEVELS

RCG Research Inc (Indianapolis, IN, (800) 442-8272) offers three levels of Spice simulator training classes to teach engineers about circuit simulation and device modeling. The beginner class introduces Spice, covers Spice controls and analysis, and concludes with an afternoon lab. The user class covers nonconvergence, time-step control, matrix manipulations, and dc and ac transient analysis. And the expert class covers device models, Monte Carlo analysis, test-pattern design, and sizing program.

All classes are one-day long and cost $240 per person. The company will teach the classes at your facility or at theirs on selected dates. The next batch of classes will be held at the company May 2, 3, and 4. For more information, contact Ron Kielkowski, Director of Training, Box 509009, Indianapolis, IN 46250.—Julie Anne Schofield

UNIX OS FOR 80386 AND 68030 µPs FITS IN ROM

Traditionally a disk- or LAN-based operating system, Unix has not often been used in stand-alone, embedded designs. LynxOS from Lynx Real-Time Systems Inc (Campbell, CA, (408) 370-2233) provides a POSIX-compliant Unix operating system for Intel's (Santa Clara, CA, (408) 987-8080) 80386 µP family that you can burn into ROM. The LynxOS kernel requires no more than 160k bytes of ROM, so you could conceivably create systems that fit into 256k bytes of ROM and need no more than 256k bytes of RAM. The ROM-based systems development kit for LynxOS/386 costs $2995 and includes a license for two target systems. A similar kit for the 68030 µP costs $4995.—Steven H Leibson

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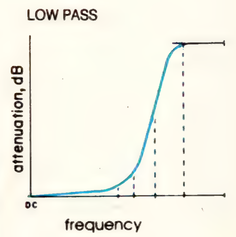

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

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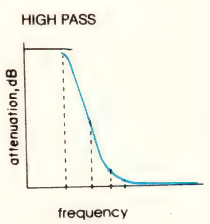
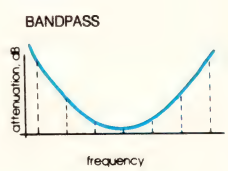


MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz



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PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

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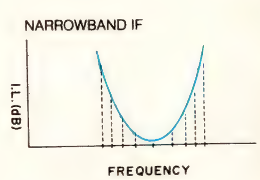

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
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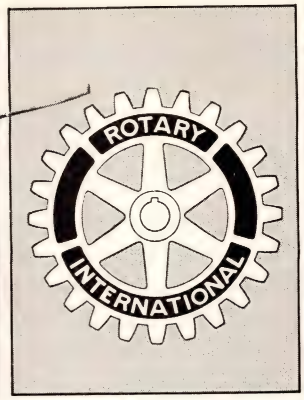

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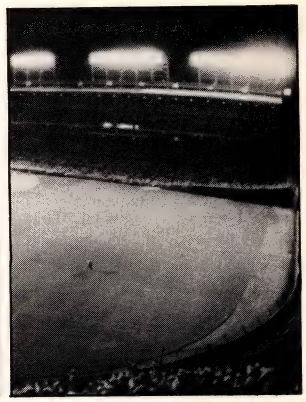

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SIGNALS & NOISE

Another view of Australian adage

In regard to Jon Titus's editorial entitled "She'll be right, mate" (EDN, October 12, 1989, pg 49), the version of the Australian saying that I'm familiar with is "She'll be right, mate, just give her a go." Far from the easy-going "Don't worry" attitude Jon equates it with, it has always seemed to represent the inspired improvisational point of view that stands out as one of the better traits human beings have. It's a compression of stoic acceptance of reality with the attitude that one will make the effort, nevertheless, using what's at hand.

Although I'm no student of Australian society myself, Jon seems to have twisted his experience [with] it to fit the point of the editorial. [Looking at Australia,] we have a society begun with a population that another society, "Mother England," considered undesirable and stranded for all practical purposes in a number of isolated settlements. These settlements in essence were "desert islands." Administrative coordination of Australia was done via London, so it's quite apparent that anything that really had to get done was done ad hoc. No more food? Well, you sure can't send out for pizza. The hamstrung bureaucracy was justifiably regarded with suspicion, and things did not improve that much by 1941 [the time of World War II]: Most of the Australian army was off helping defend the Empire, as it was in World War I.

The motion pictures *Gallipoli* and *Breaker Morant* both portray some aspects of this Australian attitude. With the increasing diversity of TV cable programming, the cable channels are also adding excellent TV documentaries from Australia. One, on "Banjo" Patterson, adds great dimension to the author of "Waltzing Matilda," itself a musical presentation of the "She'll be right" and the Australian attitude toward authority. Another, "The Last Bastion," lets you experience World War II from the Australian point of view—that is, 10,000 miles from anybody, the Japanese on the doorstep, and "Oh yes, you don't mind if we borrow your army a bit longer, do you?"

Jon's editorial also sounded a bit one-sided, regarding "surly clerks." Do we ever mistreat representatives of an offshore supplier—yell and scream at them, call them names, accuse them of cheating us? Probably not. The technical market is a fairly polite one. Now, go into a low-priced discount merchandiser where four clerks service 10 clerks' worth of customers. (Of course we go there for our blenders, why pay 30% more at a nice comfortable store with plenty of expensive labor?) In retail sales, these people are treated like cattle. They look at their humble prospects. They're liable to lose the pitiful benefits they've built up over three to five years when yet another conglomerate takes the company over. They look at what their salary will buy in the Northeast winter with two kids, day care, high rent, and an aging car. I bet they're mad as hell, but they're going to take it; what else can they do? But don't expect them to be terribly cheerful.

Name witheld by request

The implications of calling-number ID

As I read Steve Leibson's editorial, "Don't call me: I'll call you" (EDN, January 4, 1990, pg 43), I found myself in agreement until I reached the final paragraph. Technology is a double-edged sword, and calling-number ID [the phone company furnishing you with a caller's phone number before you answer the phone] is a perfect illustration of this fact.

Here is my reply to Steve: In your editorial you say, "Today, possession of your phone number is a license to invade your privacy." Since yours is not going to be the only phone using this feature, think of the number of databases that your phone number is going to go into when you call anyone for any commercial purpose. Remember the junk mail you got as a result of giving your address when you ordered something by mail? Think of the junk calls you'll get from itinerant Persian rug salesmen when you call a rug-cleaning establishment for an estimate.

The worst of it is reserved for those who have an unlisted phone number. After 50 or more calls, the only place it will be unlisted is in the phone book!

And as for its usefulness, how many phone numbers will you program into your call screening—your brother, associates at work, etc? What about the high-school classmate passing through town, the emergency call from the hospital or the Red Cross? You'll answer the phone anyway, won't you? But you say that you'll complain to the company, now that you have their number? I'm sure that your complaint will tweak the conscience of a company that deliberately calls you during dinner hour. So then you'll program to screen that number? Not good enough, because the real boiler-room operations will change phone numbers like you and I change socks.

The main thrust of your editorial seems to be against random solicitation. Calling-number ID and call screening cannot solve the problem without throwing out the baby with the bath water. It can (and will) create a host of new privacy violations.

You can't wait? I can!

Bud Couch
Portland, OR

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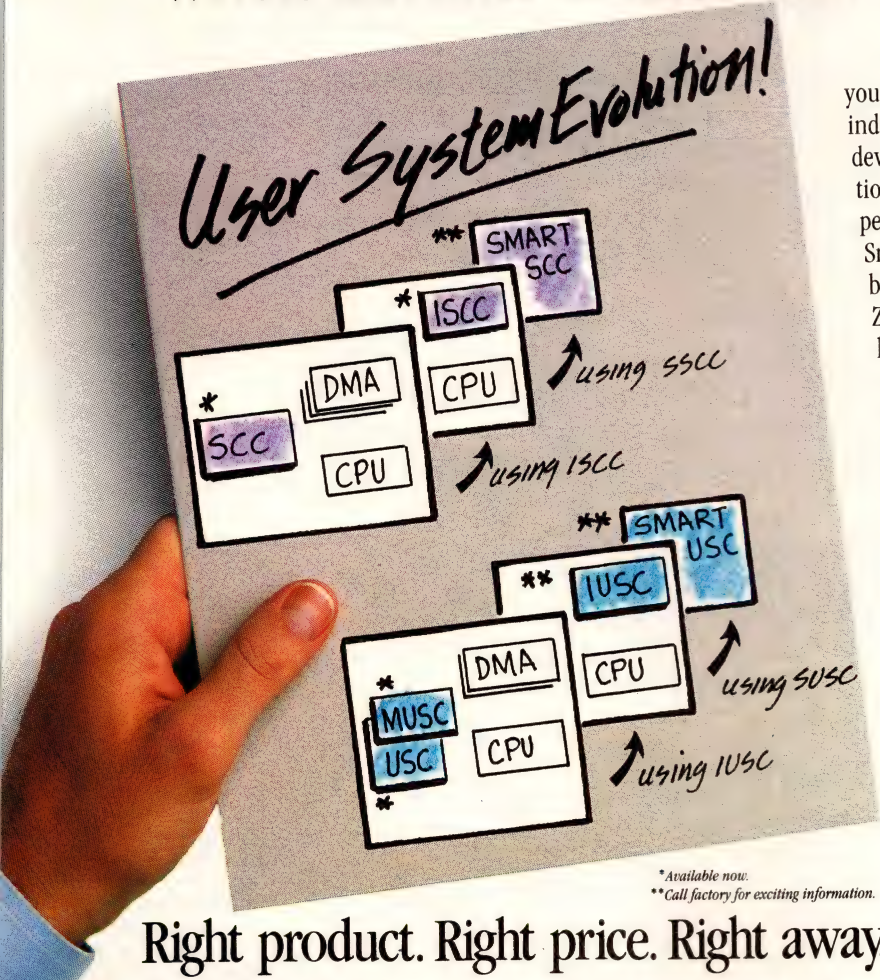

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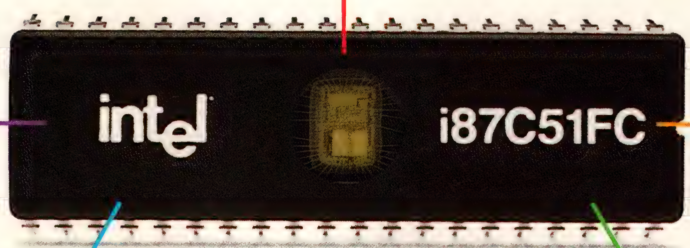

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Commercially Available RISC Processors and Workstations—Architectures and Applications, Cambridge, MA. DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. FAX (617) 969-6689. April 2 to 4.

Encapsulation of Electronic Devices and Components (short course), San Francisco, CA. The Center for Professional Advancement, Box 964, East Brunswick, NJ 08816. (201) 613-4500. FAX (201) 238-9113. April 2 to 4.

Hybrid Microcircuit Technology (short course), Bethlehem, PA. National Training Center For Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18015. (215) 861-5450. FAX (215) 861-5060. April 2 to 6.

Product Design to Pass EMC Regulations (short course), Los Angeles, CA. Interference Control Technologies, Box D, Gainesville, VA 22065. (703) 347-0030. April 3.

VHDL Users' Group 1990 Spring Meeting, Boston, MA. VHDL Users' Group, Conference Management Services, 127 Beaumont Ave, San Francisco, CA 94118. (415) 329-0510. April 4 to 6.

UNIX C++ Conference, San Francisco, CA. USENIX Conference Office, 22672 Lambert St, Suite 613, El Toro, CA 92630. (714) 588-8649. April 9 to 11.

C Programming Workshop (short course), Seattle, WA. Specialized Systems Consultants Inc, Box

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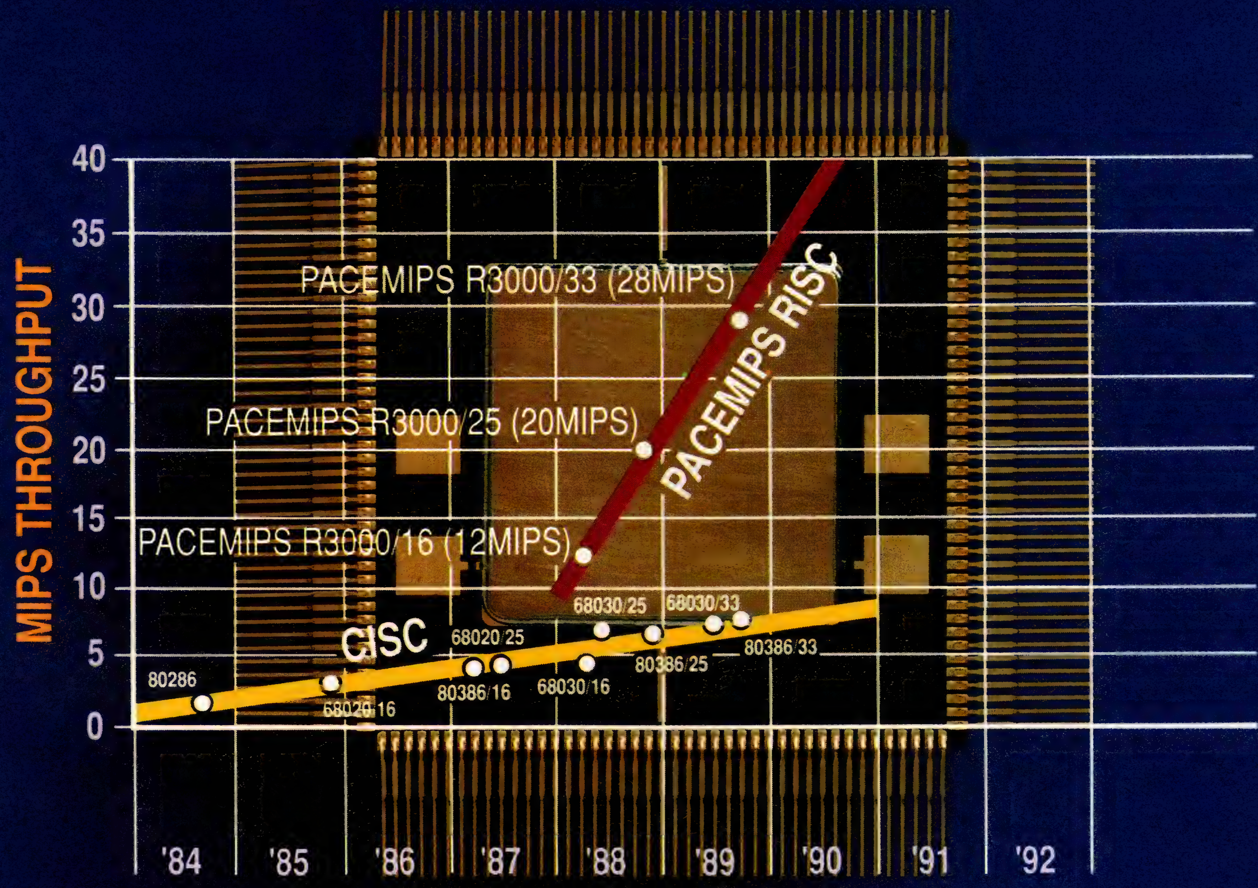

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55549, Seattle, WA 98155. (206) 527-3385. FAX (206) 527-2806. April 9 to 13.

IEEE VLSI Test Workshop, Atlantic City, NJ. Wesley Radcliffe, IEEE Computer Society, IBM E Fishkill, Dept 277, Bldg 321-5E1, Hopewell Junction, NY 12533. (914) 894-4346. FAX (914) 892-6790. April 10 to 11.

Surface Mount (SMT)/Fine Pitch (FPT) Design and Manufacturing Techniques (short course), Sunnyvale, CA. PPM Associates, Box 700039, San Jose, CA 95170. (408) 996-9765. April 10 to 11.

1990 Technical Symposium on Optical Engineering and Photonics in Aerospace Sensing/Exhibit, Orlando, FL. SPIE, The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX (206) 647-1445. April 16 to 20.

DOD-STD 2167A/2168, San Diego, CA. David Maibor Associates Inc, Box 846, Needham Heights, MA 02194. (617) 449-6554. April 17 to 19.

Electronics Packaging Technology (short course), East Brunswick, NJ. The Center for Professional Advancement, Box H, East Brunswick, NJ 08816. (201) 613-4500. FAX (201) 238-9113. April 23 to 25.

Integrated Circuit Manufacturing Technology (short course), San Francisco, CA. The Center for Professional Advancement, Box H, East Brunswick, NJ 08816. (201) 613-4500. FAX (201) 238-9113. April 30 to May 2.

Structured Development Forum XI, San Diego, CA. Computer Sciences Corp, 1321 Mercedes Dr, Hanover, MD 21076. (301) 859-0400. April 30 to May 3.

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MECHANICAL SHOCK	1.5Kg's, 0.5μsec pulse	883, Method 2002
VIBRATION	variable frequency 20 to 2,000 Hz	750, Method 2056
TEMPERATURE CYCLE	-65°C to +125°C 200 cycles, 10 min. dwell	883, Method 1010
AUTOCLAVE (pressure pot)	14.7psi, T_A +121°C, 96 hr.	H-P GSS, 09-109
85/85	85°C @ 85% humidity 168 hr., no bias	H-P GSS, 09-107B
ACCELERATED HI-TEMPERATURE STORAGE	300°C, 325°C, 350°C storage until 50% failures	883, Method 1008

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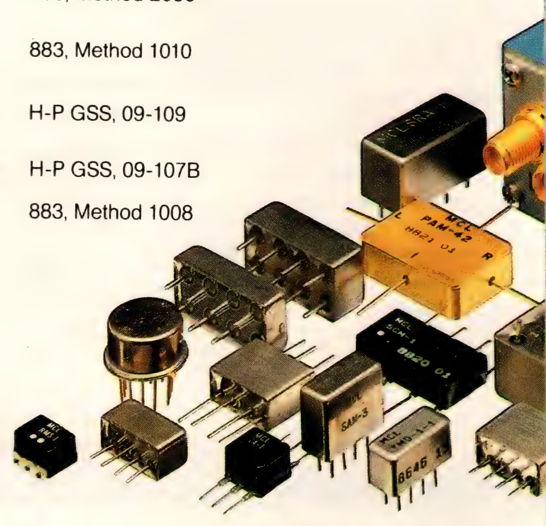

F130-1 REV. A

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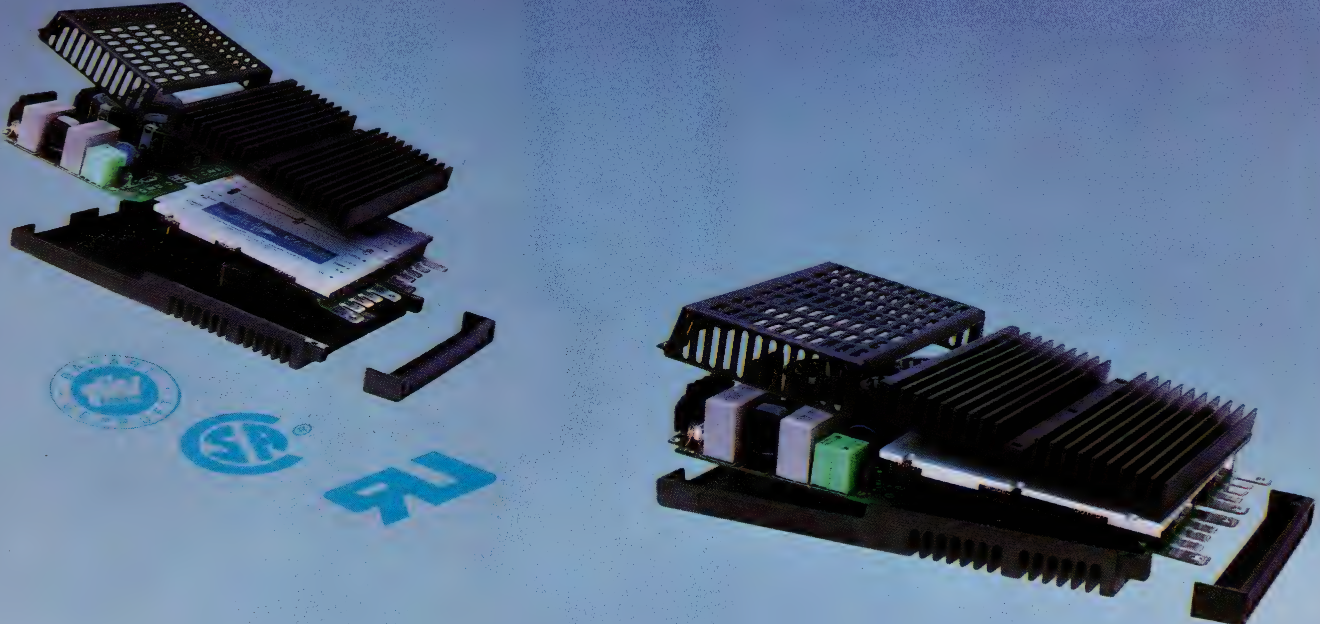

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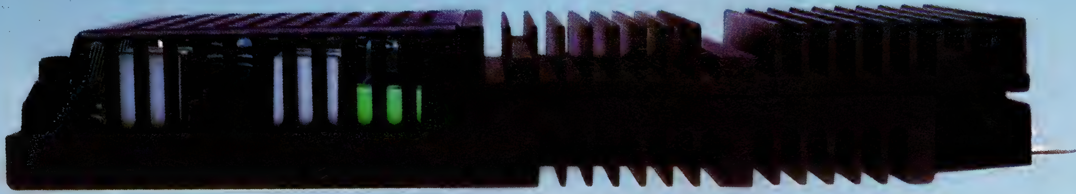

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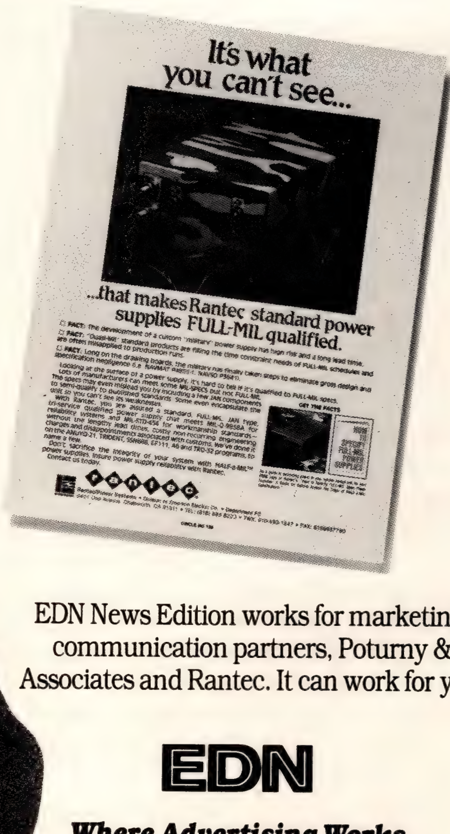

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CIRCLE NO. 36

Thanks, but no memories

Many people are mourning the death of the US Memories consortium, a group trying to establish a US source of DRAMs. They say that the failure of the US Memories venture is another symptom of myopia in US companies. It's not. Left to their own devices, US companies are smarter than some people think. Instead of emulating the large Japanese companies and cartels, US companies will remain competitive by going the helter-skelter ways of start ups and spinoffs.

The source of DRAM supplies is an emotional issue, so let's tackle the argument that Japanese suppliers will establish a headlock on the DRAM market without competition from US Memories. That's nonsense. Years ago, US companies had the lock on DRAM markets, *and they let it dribble away to Japanese competitors.* These same US companies could get back into the DRAM market now, but few have the will to do so. It's unlikely than a consortium would add the needed backbone, even though IBM is now willing to license its DRAM technology to US manufacturers. Samsung, a Korean manufacturer, is ready to challenge the Japanese DRAM manufacturers, and a few US manufacturers are still in the DRAM business. I'm confident that there will be plenty of DRAMs from enough manufacturers to guarantee supplies for all OEMs.

Some people argue that manufacturers of the advanced DRAMs gain critical knowledge of advanced semiconductor-processing techniques. That's true. But many advances in electronics will come from areas that don't depend on the latest DRAM technology—for example, high-performance op amps, neural-net chips, or signal-processing ICs. So DRAM technology may beget better DRAMs, but it doesn't always mean supremacy in other products.

Overall, we'll find that US semiconductor firms have lost little by bowing out of a noncompetitive, single-source memory venture. In my opinion, the future belongs to smaller competitive companies that customize products to customers' needs. You can't do that with DRAMs. Companies that are strong competitors and that react quickly to the vagaries of markets will be in ascendancy. But companies that offer commodity products and compete on price instead of value are doomed.

In light of US Memories' death, Sony's chairman Akio Morita is surprised that US companies would not adopt the bigger-is-better attitude of Japanese companies. He cannot understand that size is often irrelevant. Instead of mourning the loss of US Memories, let's make sure that government rules and regulations don't stifle competition and don't tax our businesses out of existence. Companies whose products embody ingenuity and innovation can take on a large, slow-moving company any day. If they couldn't, relative newcomers such as Compaq, Cypress Semiconductor, and Sun Microsystems wouldn't exist.

Jon Titus

Jon Titus
Editor

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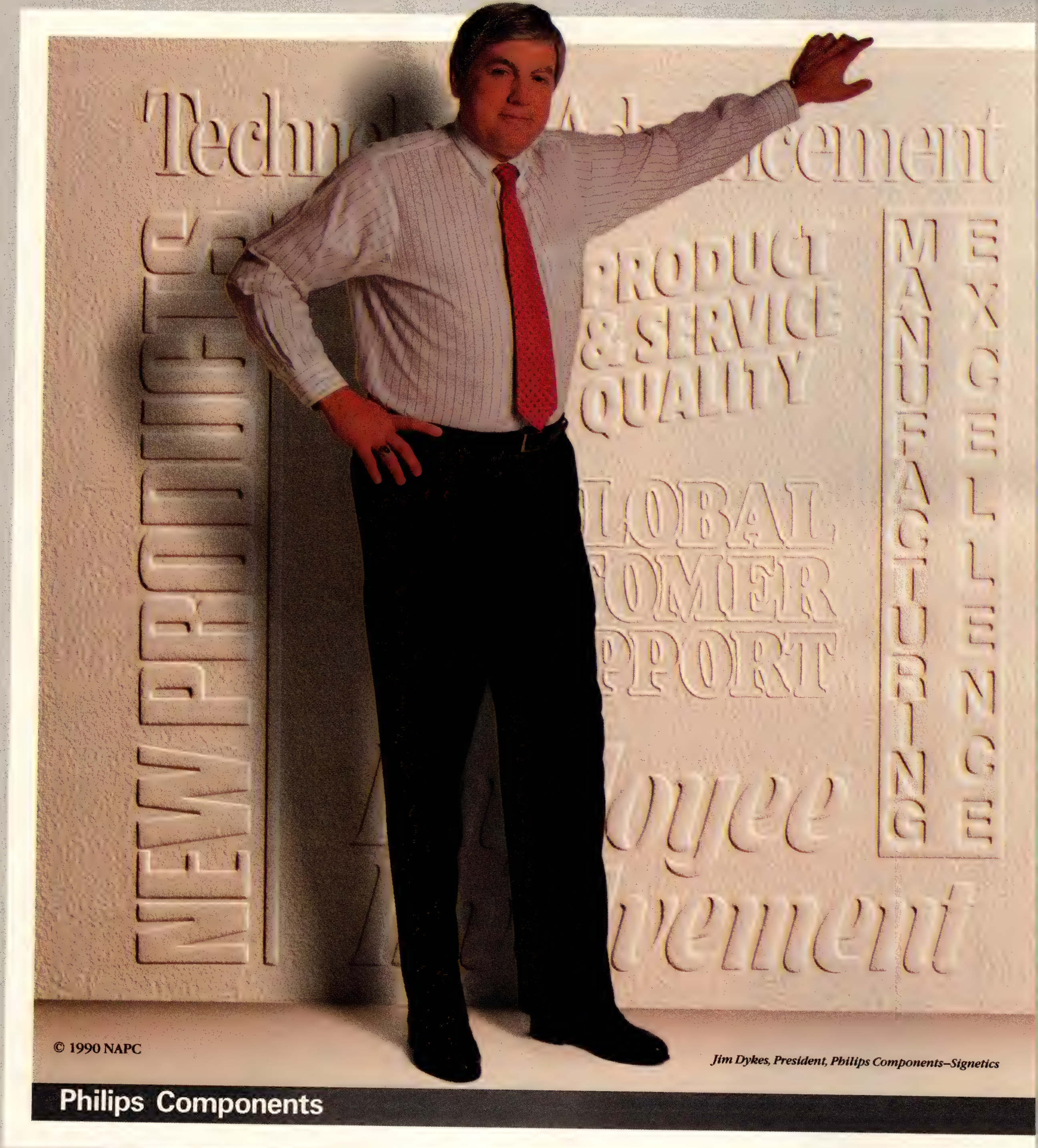

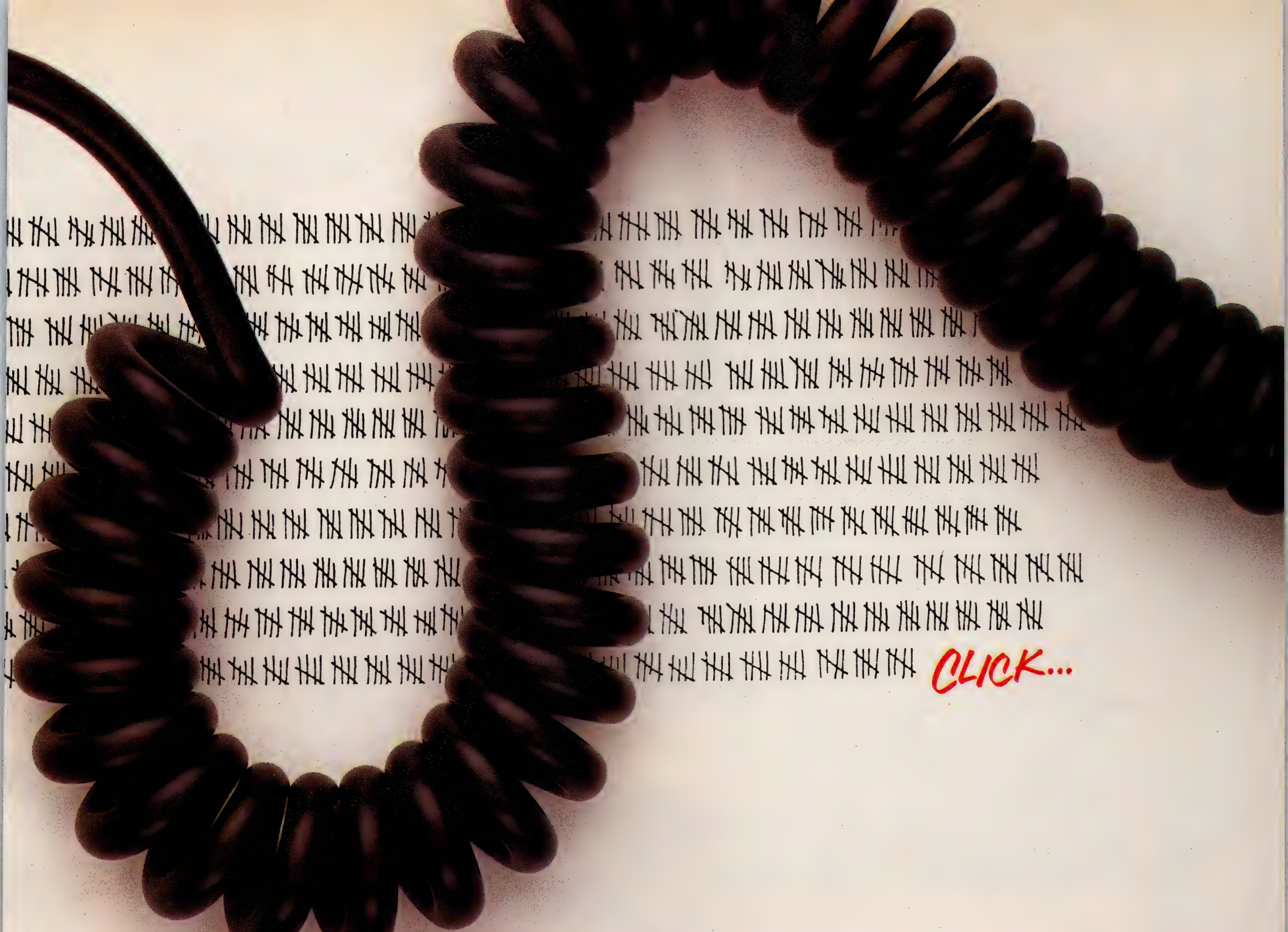
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MULTICHANNEL SAMPLING ADCs

ICs and hybrids pose as entire systems

Consider using multichannel sampling ADCs—if they meet your flexibility and performance needs.

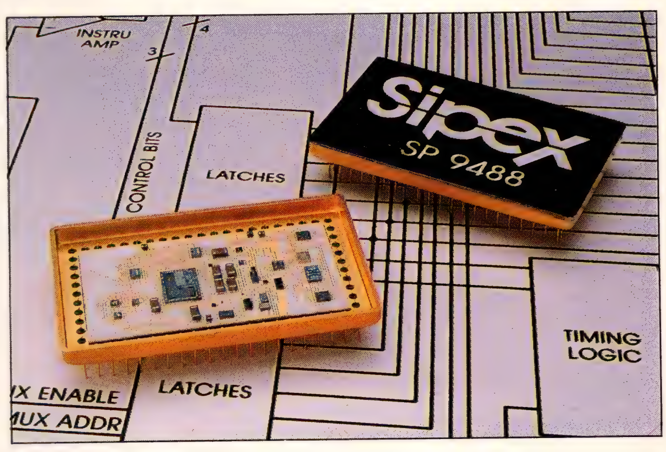
Anne Watson Swager,
Associate Editor

The benefit of using highly integrated ICs is pure and simple: They do more of your work for you. This benefit is especially true of the analog front end of data-acquisition systems. ICs and hybrids that combine a multiplexer, a S/H amplifier, and an ADC reduce the time and effort you would otherwise devote to sensitive analog design. Not only do these chips free you from designing each analog stage, they shift the burden of testing—and guaranteeing—the entire system to the manufacturer.

However, these multichannel sampling ADCs may lack an important feature or not be flexible enough for your system. You have to decide what combination of features and performance is most cost-effective for your design. For example, there are some devices with, and some devices without, voltage references. If an IC or hybrid has an internal reference, it may not have the precision necessary for your application. Consider whether a less highly integrated part and a few more external components might help your system achieve higher performance. (See **box,** "Board and box vendors make surprising choices.")

Most converter manufacturers agree that a multiplexer, a S/H amplifier, and an ADC are the basic components of any data-acquisition system. (Keep in mind that these devices are only a subset of a large number and variety of data-acquisition components.) Beyond these components, a device can have all sorts of bells and whistles. The multichannel sampling ADCs in **Table 1** have at least a 2-channel multiplexer, a S/H amplifier, and an A/D converter in the same package. In some cases, the ICs and hybrids include more subcomponents, such as instrumentation amplifiers, voltage references, and internal clocks. These products are a mixture of industry-standard hybrids—such as Datel's HDAS-8/16—and 1-year-old monolithics—such as Linear Technology's LTC1290.

Most of these ICs and hybrids are successive-approximation types. Although some low-frequency applications don't require the sample-and-hold function, most of these parts require S/H amplifiers to accurately digitize signals at sampling rates close to the ADC's Nyquist limits. A few of the ICs are half-flash



ICs and hybrids that combine a multiplexer, a S/H amplifier, and an ADC *are just a subset of an increasing market of data-acquisition components that offer more functions per package. Hybrids, such as Sipex's SP9488, offer you the most complete set of functions, but ICs feature lower prices.*

converters. **Table 1** also features one single-slope converter from Fujitsu. The company recently released a variety of other multichannel ADCs without internal S/H amplifiers for low-frequency applications.

Hybrid devices are the most complete data-acquisition system in a single package. For many military applications, the reliability of the single package overcomes a hybrid package's higher cost. And despite the emergence of inexpensive ICs, hybrid manufacturers are actively pursuing new designs. For example, Datel has introduced three products in the last six months.

In addition to featuring the highest throughputs—the HDAS-524 and -528 run at 400 kHz—the newer

Table 1—Representative multichannel sampling ADCs

Manufacturer	Part number	Resolution (bits)	Throughput/ conversion time	Maximum linearity error	Input channels	Input range (V)
Analog Devices	AD1334	12	67 kHz	±1 LSB	4 SE	±5
	AD7824/28	8	100/50 kHz	±½ LSB	4/8 SE	0 to 5
Burr-Brown	SDM862/3	12	33 kHz	0.012% FSR	16 SE/8 DI	0 to 10, ±5, ±10
	SDM872/3	12	50 kHz	0.012% FSR	16 SE/8 DI	0 to 10 ±5, ±10
Datel	HDAS-8/16	12	50 kHz	±¾ LSB	8 DI/16 SE	±0.1 to ±10
	HDAS-75/76	12	75 kHz	±¾ LSB	8 SE/4 DI	±0.1 to ±10
	HDAS-524/8	12	400 kHz	±¾ LSB	4 DI/8 SE	±0.1 to ±10
	HDAS 950/951	16	75 kHz	±½ LSB at 14 bits	8 SE/4 DI	±0.1 to ±10
Fujitsu	MB4053/63	8	300 μsec	±0.2%	6 SE	0 to 5
Linear Technology	LTC1090	10	30 kHz	±½ LSB	4 DI/8 SE	0 to 5, 0 to 10, ±5
	LTC1091/3/4	10	20 μsec	±½ LSB	2/6/8 DI and SE	0 to 5, 0 to 10, ±5
	LTC1095	10	25 kHz	±½ LSB	6 SE or DI combinations	0 to 5
	LTC1290	12	50 kHz	±½ LSB	4 DI/8 SE or combinations	0 to 5, ±5
	LTC1294	12	13 μsec	±½ LSB	8 SE	0 to 5, 0 to 10, ±5
Maxim	MAX154/158	8	2.5 μsec	±½ LSB*	4/8 SE	0 to 5
Micro Linear	ML2200/08	12+	31.5 μsec	±½ LSB	4 DI/8 SE	±5
Micro Networks	MN7145/6/7	12	25 kHz	±½ LSB	8 SE	0 to 10/±5/±10
	MN7150-8/-16	12	50 kHz	±½ LSB	8 DI/16 SE	±0.01 to ±10
National Semiconductor	ADC08032/4/8	8	8 μsec	±½ LSB*	2/4/8 SE	0 to 5
	ADC1034/38	10	13.7 μsec	±½ LSB*	4/8 SE	0 to 5
Sipex	SP9462/3	12	33 kHz	±0.024% FSR	16 SE/8 DI	0 to 10, ±5, ±10
	SP9480	16	25 kHz	±0.003% FSR	8 SE	0 to 10, ±10
	SP9488	16	50 kHz	±0.003% FSR	8 DI or 16 SE	0 to 2.5, 5 or 10, ±2.5, ±5, ±11
Texas Instruments	TLC1540	10	32 kHz	±½ LSB	11 SE	0 to 5

Notes: DI = Differential.
SE = Single Ended.
NS = Not Specified.
FSR = Full-Scale Range.
NA = Not Applicable.
DDIP = Double-Wide DIP.
*Spec is total unadjusted error.
Each converter requires ±15 and 5V supplies unless otherwise specified.

hybrids require much less power and space than their predecessors. The HDAS-75 and -76 75-kHz hybrids dissipate 500 mW typ. Three other manufacturers deserve mention for their ability to pack functions into small packages. Burr-Brown's SDM86x/87x 33- and 50-kHz devices come in surface-mount LCCs. Sipex's 12-bit SP9462 and -9463 come in 16-pin PGA (pin grid array) packages, and Micro Networks' MN714x family comes in 28-pin double-wide DIPs.

The highest performance you'll find in these hybrids and ICs is 14 bits. Sipex was the first to feature 14-bit linear devices, the SP9480 and -9488. The SP9488 is an enhanced version of the -9480 with twice the speed and more input-

Input protection	Maximum power dissipation (mW)	Package	Output interface	Price (100s)	Comments
NS	1250	40-pin hybrid DIP	Parallel	$180	Tailored to DSP. Includes –5V precision reference.
None	100	24-/28-pin DIP 28-pin LCC or PLCC	Parallel	$148.6	Single 5V supply. Half-flash conversion technique.
To ±35V	1400	68-pin hybrid LCC or PGA	Parallel	$103.68	Eurocard evaluation board available. Devices include instrumentation amps and feature serial and overlap operation modes.
To ±35V	1400	68-pin hybrid LCC or PGA	Parallel	$119.23	
To ±35V	1750	62-pin hybrid package	Parallel	$235	All the company's devices include instrumentation amps, internal clocks, and 10V references except the HDAS-950/951, which has a 5V reference.
To ±25V	700	40-pin hybrid DDIP	Parallel	$116	
To ±25V	3000	40-pin hybrid DIP	Parallel	$281	
To ±25V	1400	40-pin hybrid DDIP	Parallel	$293	
To 30V	50	16-pin DIP or flat package	NA	$2.32/$2.95 (1000)	Single 5-to-15V supply. Single-slope converter; μP provides addressing, counting, and timing functions.
None	12.5 (V_{CC}=5V)	20-pin DIP	Serial	$9.90	±5, 5, or 10V supply
None	12.5 (V_{CC}=5V)	8/16/20-pin DIP	Serial	$9.90	±5, 5, or 10V supply.
None	23.5 (V_{CC}=5V)	18-pin DIP	Serial	$12	Includes 5V buried-zener reference. Single or split supplies.
None	25 (typ, V_{CC}=5V)	20-pin DIP	Serial	$15.95	5V or ±5V supply. Features low-power mode.
None	25 (typ, V_{CC}=5V)	20-pin DIP	Serial	$12.95	
None	75	24-/28-pin DIP and SO packages	Parallel	$10.45/$10.95	Half-flash conversion technique. Single 5V supply. Includes 2.5V reference.
To ±12V	400	40-pin DIP	Parallel	$41/$43	Requires ±5V supplies. Includes 2.5V references.
To ±35V	1000	28-pin hybrid DDIP	Parallel	$89	Internal ADC clock and reference.
To ±35V	2300	62-pin hybrid DIP	Parallel	$248	Includes 10V reference.
None	20	8-pin/14-pin/20-pin DIP	Serial	$5/$5.50/$5.95	Single 5V supply, on-chip 2.6V reference.
None	20	16-pin/20-pin	Serial	$9.50	Single 5V supply.
To ±35V	1400	68-pin hybrid PGA	Parallel	$100	Includes instrumentation amp and reference.
To ±35V	1200	32-pin hybrid DDIP	Parallel	$229	Streamlined version of SP9488.
To ±35V	1400	62-pin hybrid DDIP	Parallel	$399	Self-calibrating converter with instrumentation amp and reference.
None	12.5	20-pin DIP	Serial	$6.99 (1000)	S/H amplifier is software-controllable. Internal self-test voltage.

and output-interface options. Datel recently joined this high-resolution market with its HDAS-950 and -951.

Some hybrids also have features that are particularly important to signal processing. Analog Devices tests and specifies AD1334s for a S/N ratio and THD of 70 and −76 dB, respectively. The input structure of the AD1334 differs from the other all-in-one hybrids. Instead of a multiplexer and a single S/H amplifier, the device includes four dedicated S/H amplifiers and a 4:1 multiplexer.

While hybrid manufacturers continue to develop new products, the monolithic camp is equally busy. New 10- and 12-bit monolithic devices from National Semiconductor and Linear Technology provide competitive performance and flexibility for low costs. These serial-interface devices typically have separate conversion and I/O clocks, which simplifies μP control. The LTC1090 and -1290 let you program the input range, the input type, and the data sequence (MSB or LSB first).

The linearity specifications of many of these multichannel ICs and hybrids can compete with those of stand-alone ADCs. Most of the ICs that have linearity ratings of ½ LSB are also available in 1-LSB versions. Many manufacturers guarantee a device's performance over temperature. Datel specifies linearity over the entire temperature and power-supply ranges.

One newer specification IC manufacturers often quote is total unadjusted error. Total unadjusted error compares the performance of the actual ADC to an ideal converter without any necessary external ad-

Board and box vendors make surprising choices

Many designers whom you'd expect to use highly integrated ICs due to space considerations don't. One box-level and three data-acquisition-board manufacturers prefer monolithic multiplexers, S/H amplifiers, and ADCs to both hybrid and monolithic multichannel sampling ADCs. Instead of moving toward using more system ICs, Audrey Harvey of National Instruments (Austin, TX) says her company is moving in the opposite direction. Its engineers are designing S/H amplifiers of their own.

Data-acquisition-board manufacturers don't use these highly integrated devices mostly because of the requirements of their largest customer: scientific research-and-development labs. These manufacturers do sell boards for industrial environments, but scientific equipment has some requirements that other systems don't. Although your system may not have these same requirements, the following product-selection criteria should make you stop and think.

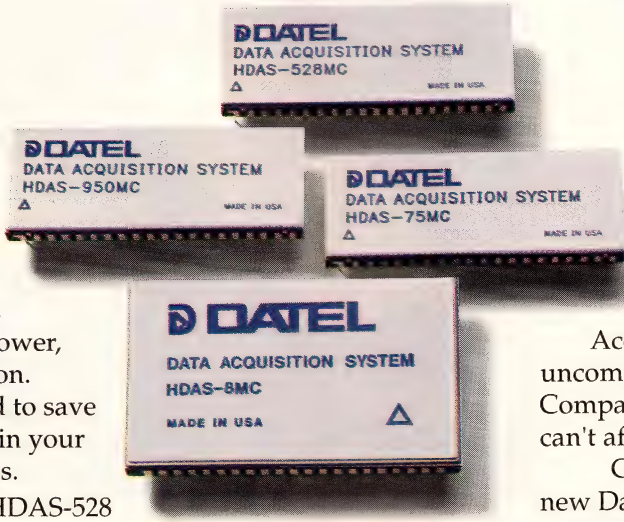
One of the primary reasons data-acquisition-board manufacturers use or don't use a certain type of component is cost. These manufacturers don't even look at hybrid products. In many cases, they have experienced analog designers, so the costs of generating comparable designs are not high. Many data-acquisition-board manufacturers say they'll take a look at the low-cost monolithic all-in-one ICs, but they don't seem to be in any great hurry to find specific product applications for these devices. Apparently, their current design methods meet their projected goals.

Board and box manufacturers also require certain levels of performance. They tend to look only at ICs with 12 or more bits of resolution. I/O Tech (Cleveland, OH) manufactures IEEE-488 box-level products with 16-bit resolutions. According to Don Ecker, designer of the company's ADC488, it's hard enough to find a true 16-bit converter, let alone one packaged with additional circuitry.

The flexibility of both the input structure and the μP interface also affects product selection. Steve Conners of Data Translation (Marlboro, MA) cites the lack of user-selectable inputs and restricted input ranges as major disadvantages of hybrids and monolithics, respectively. Most scientific laboratory instruments have ±10V ranges, thus making some of the inexpensive 0-to-5V monolithics unacceptable. However, this lower-input range is not a disadvantage for industrial or automotive applications. Current loops of 4 to 20 mA with impedances of 250Ω require only 1 to 5V. Barry Phillips of MetraByte (Taunton, MA), another data-acquisition-board manufacturer, points out some triggering limitations of these all-in-one ADCs. Many of these devices operate when the μP triggers the ADC as a memory-read or -write operation. "These bus-only devices are inflexible," says Phillips.

None of these concerns may directly apply to your system, but they point out some basics of product development: Know your customers and the specifications they want, know your cost limitations, and know the value of your competitive edge. Choose the right parts to get the job done.

DATEL Data Acquisition Systems when you can't afford compromise



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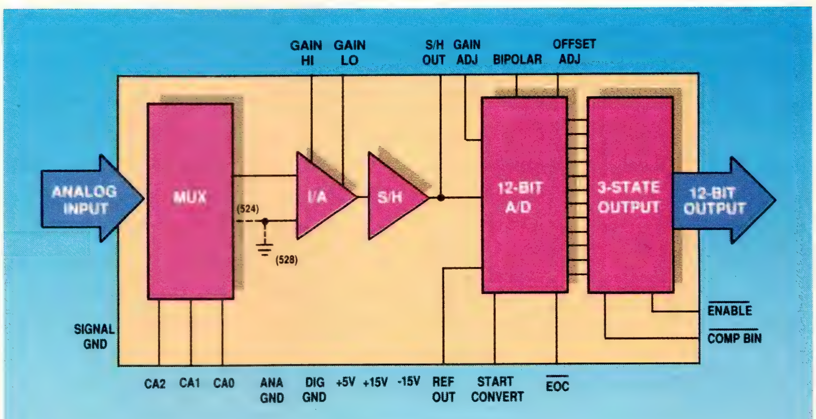

HDAS-524/528 Block Diagram

Model	Bits	Throughput (KHz)	Power (Watts)	Channels	Package
DAS-952R	8	17	0.015	16 SE	40-PIN DIP
HDAS-16/8	12	50	1.45	16 SE/ 8D	62-PIN Hybrid
HDAS-75/76	12	75	0.500	8 SE/ 4D	40-PIN DDIP
HDAS-534/538	12	150	2.6	4 SE/ 8D	40-PIN DDIP
HDAS-524/528	12	400	2.6	8 SE/ 4D	40-PIN DDIP
HDAS-950/951	16	75	1.1	8 SE/ 4D	40-PIN DDIP

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justments. The use of a total-error specification is not unique to all-in-one ICs—you'll also find it on some stand-alone-ADC data sheets. In the case of multichannel sampling ADCs, total unadjusted error includes multiplexer and sampling errors in addition to linearity, gain, and offset errors.

National Semiconductor's ADC-0803x and ADC103x families as well as Maxim's 154 and 158 series have total unadjusted errors of ½ LSB. (These specifications appear in the maximum linearity column of the **table**.) Linear Technology and Texas Instruments provide the other error specifications in addition to the total unadjusted errors of ±½ LSB on their data sheets. Micro Linear breaks up the ML2200's and -2208's total error specifications. These devices have a maximum unadjusted zero error and a maximum unadjusted positive and negative full-scale error of ±1 LSB with an external reference.

***Hybrid manufacturers continue to develop** all-in-one packages that offer variations in speed, power consumption, and size. Datel's 40-pin HDAS-524 and -528 hybrids have throughputs of 400 kHz and dissipate 3W max.*

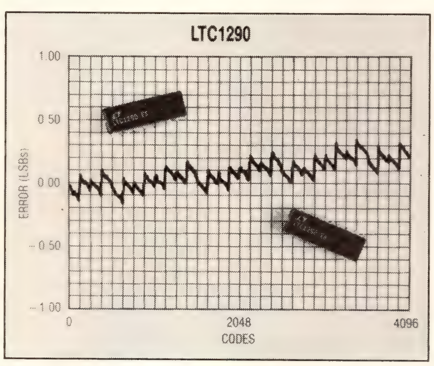
How fast is fast?

The fastest throughput of any of these ICs or hybrids is 400 kHz. Most of the other 12-bit devices have throughputs between 25 and 75 kHz. The numbers quoted are the maximum throughputs attainable for each device with any single channel running alone.

To determine the throughput of your entire system, you typically divide the device's maximum per-channel throughput rate by the number of input channels. This calculation may seem straightforward, but it often isn't. The device's throughput can change depending on the operating mode. The AD1334's 4-channel sampling rate is actually higher than the single-channel rate divided by 4. Burr-Brown's SDM family has conversion times of 45 μsec in serial mode and 30 μsec in overlap mode. In other cases, the total throughput may be lower than you would expect. If a device's per-channel throughput specification does not include channel-switching and settling times, you must add them to the total system throughput.

Always keep in mind that throughput does not equal the inverse of conversion time. If a data sheet only gives the conversion time, you have to add that number to the acquisition time of the S/H amplifier and the settling time of the input multiplexer to determine the maximum throughput rate.

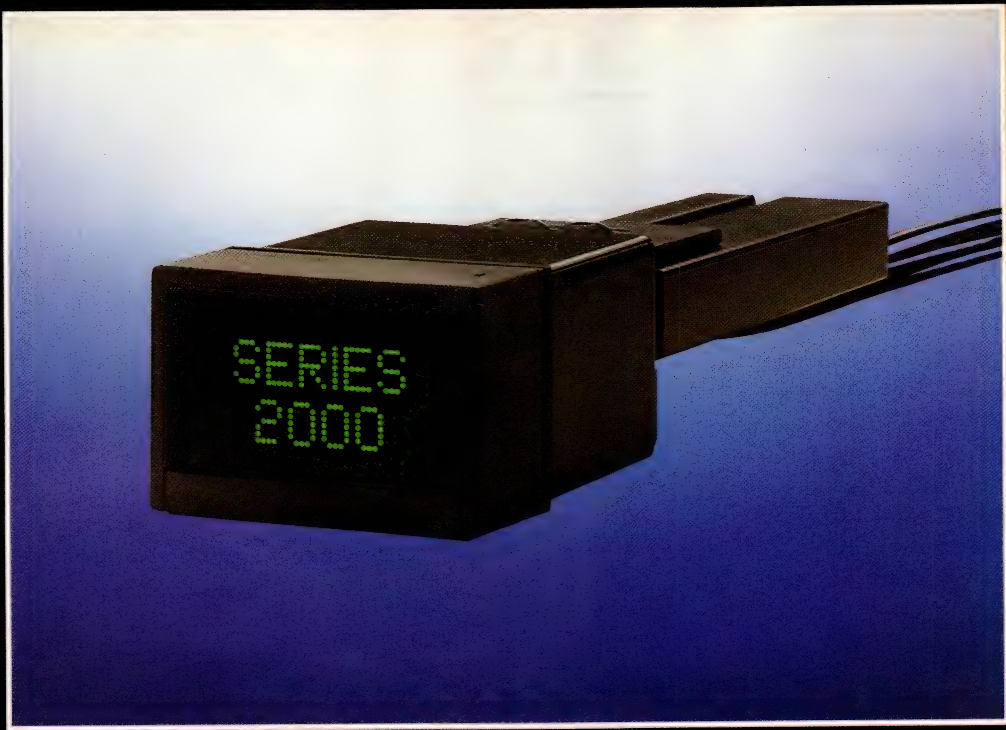
The type of output interface is one reason manufacturers specify the timing of some devices differently from others. Most hybrids have parallel interfaces and most monolithics have serial ones because of the number of output pins. Parallel-interface devices typically have 3-state outputs and a few μP control lines. Serial interfaces usually consist of a few lines directly connected to the μP's chip-select, clock, and data lines.



***The maximum linearity** of many of these system ICs is ±1/2 LSB. (Photo courtesy Linear Technology Corp)*

Willie Rempfer, designer of Linear Technology's LTC1090, says that the throughput of a serial-interface device is much more dependent on the μP's transfer rate than is the throughput of a parallel device. Thus, the company quotes specifications in clock frequencies rather than in real numbers. For example, the 50-kHz maximum throughput of the LTC1290 is really the result of the calculation: 12×SCLK+56×ACLK, where SCLK is the inverse of the μP's shift-clock frequency and ACLK is the inverse of the ADC clock frequency.

In addition to performance, another benefit—or drawback—of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Multichannel sampling ADCs

multichannel sampling ADCs is the flexibility of their input structures. Most hybrids have either single-ended or differential dedicated inputs. The SP9488 is one exception. You select among 16 single-ended channels or eight differential channels by connecting certain input pins.

Only the LTC1090 and LTC1290 series feature differential inputs in a monolithic device. You can program these inputs on the fly by setting and clearing the desired bits of the address byte from the μP. However, the switched-capacitor input of these devices (**Fig 1**) adds a few quirks to these ICs' differential operation: The ICs can accept two input signals, but the signals can't be moving relative to one another. The S/H function only applies to the plus input.

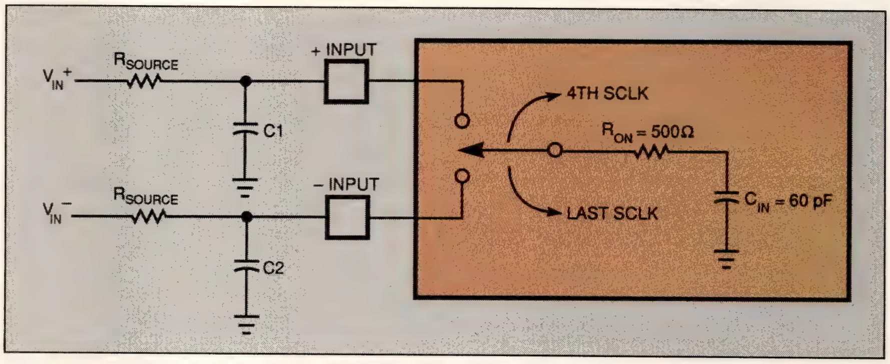

***Fig 1—The switched-capacitor input structure** of the LTC1090 and -1290 provides the sample-and-hold function on the plus input only. To maintain accuracy, the minus input must remain stable during the entire conversion.*

When C_{IN} of **Fig 1** switches to the minus input—the time when sampling occurs—its charge injects into the summing junction of an op amp. The capacitor's input stays connected to the minus input during the duration of the conversion. If the signal connected to the minus input hasn't settled or is unstable, the conversion won't be accurate. Since one input must be a fixed dc level, these inputs aren't truly differential. However, the company says that many customers use the minus input to intentionally offset the converter's input range. The ability to add offset is useful when the sensor's dc output range doesn't match the input range of the ADC.

Although these highly integrated devices have the nickname of all-in-one ICs, no device can truly fit that description. These multichannel sampling ADCs require the same grounding and bypassing techniques that are crucial to any ADC's performance. And you may have to add external components to provide

For more information . . .

For more information on the multichannel sampling ADCs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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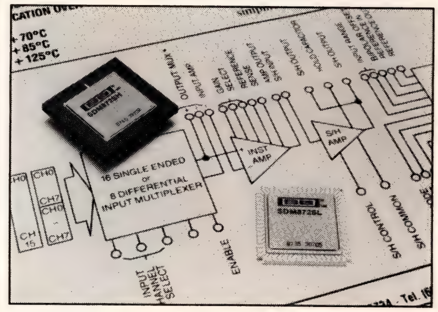
Multichannel sampling ADCs

input overvoltage protection. Most of the hybrids protect the inputs to between 10 and 15V beyond the supply voltages; they usually incorporate overvoltage-protected multiplexers. The monolithic ML2200 and -2208's inputs can go as high as 7V above the supply voltage.



***Multiple functions in a small package** is the primary benefit of any highly integrated device. Burr-Brown's SDM series packs a multiplexer, a S/H amplifier, an ADC, and more into a 1-in.² pin-grid array or LCC.*

However, the other monolithics have no such protection, so you'd have to add external clamp circuits.

Whether you're looking for the most complete system or a particular set of functions in one package, there's no question that using these ICs and hybrids will speed design time and save space in the process. Whether they offer the right combination of performance and flexibility is a question you can answer only through data-sheet scrutiny and a thorough knowledge of your design goals. EDN

Reference

1. Conner, Doug, "Analog switches and multiplexers," *EDN*, March 15, 1990, pg 130.

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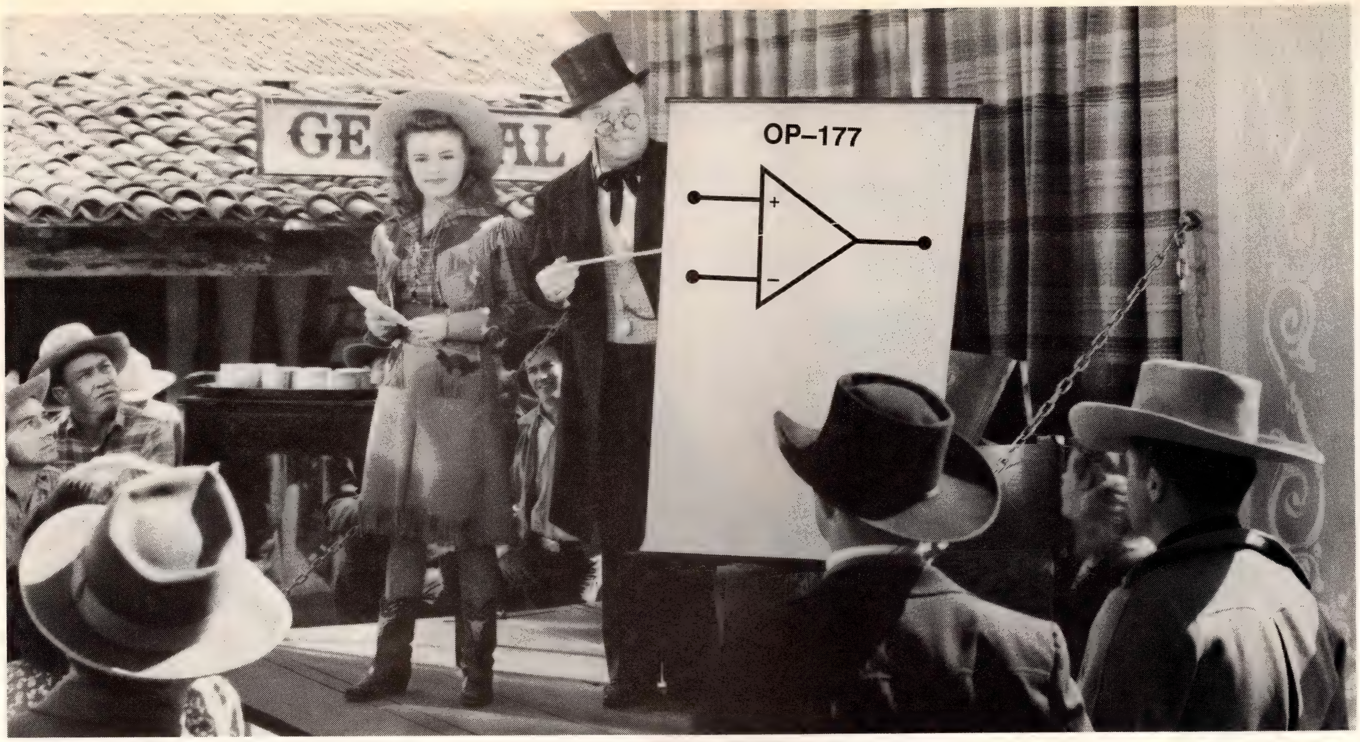

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The TMS320C25

- The TMS320C25 takes more than three times as long to compute the same size FFT, while it devours over 47k bytes of memory.[1]
- The TMS320C25 is limited to one access of external data every two cycles.
- The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
- The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD >FF03,* –. While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

We're not saying the TMS320C25 is slow. But even if it were twice as efficient as it is now, it'd still be a lot slower at DSP than the ADSP-2100. The fact is, the ADSP-2100 is out in front of the TMS320C25 in performance, readability of code, and development tools.

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[1] EDN, "EDN's DSP Benchmarks," September 29, 1988.

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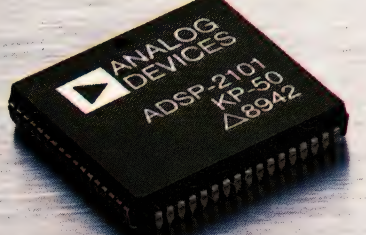

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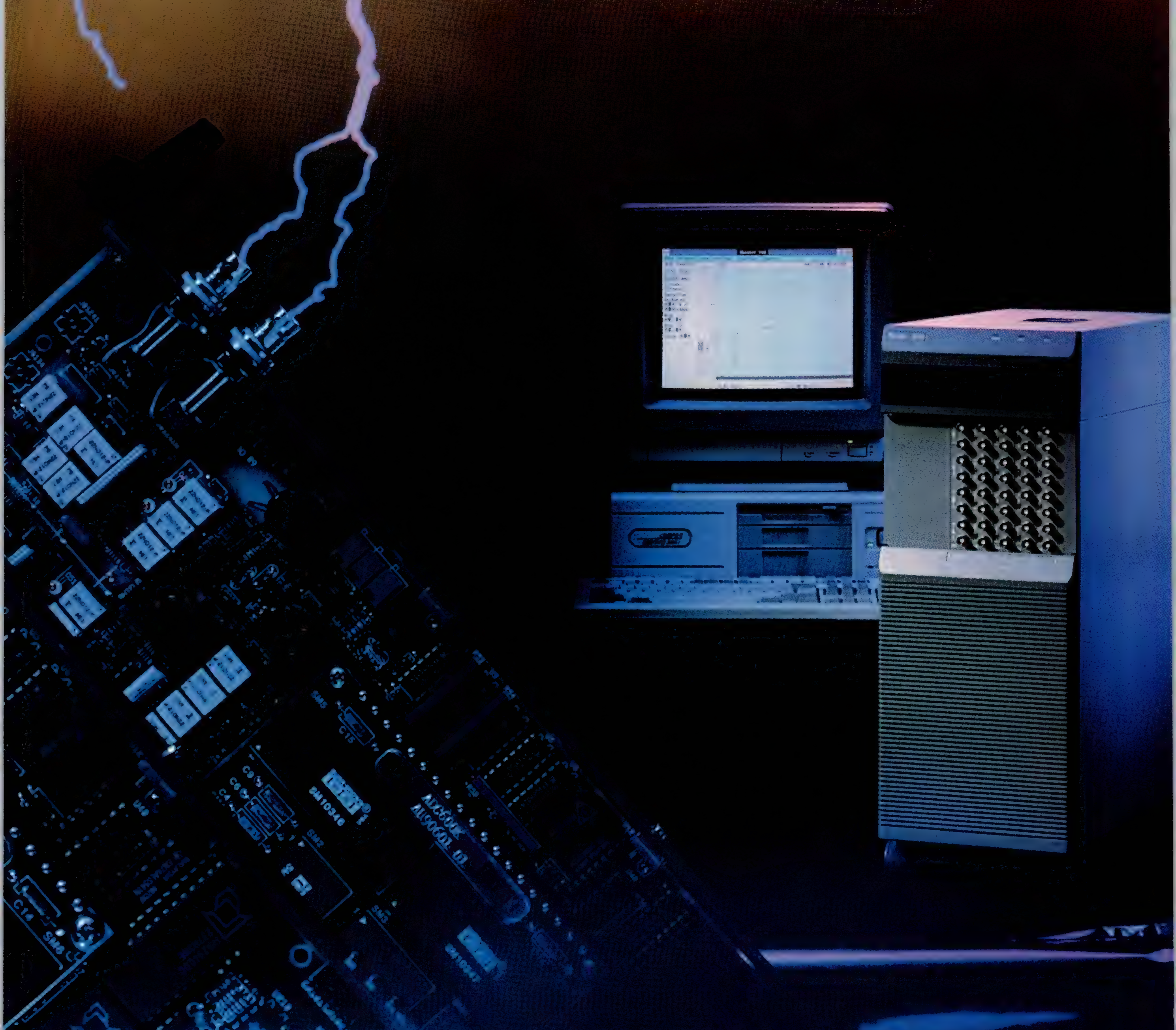
CIRCLE NO. 49

THE WAVE OF THE FUTURE



Rise above any waveform measurement challenge with the new Nicolet System 500.

It's the most powerful and flexible digital waveform acquisition system available. With more channels. More speed. More memory. Greater resolution. And in the optimum configuration, starting as low as $1,645 per channel.

Available in portable or rack mount, this premier *turnkey* system features:

Independent digitizer boards with maximum sampling rates of up to 10 MS/s.

Multichannel flexibility. Whether it's two or 200 channels, the 500 can handle it.

Local processing. Lightning-fast on board calculation capabilities save you time.

And . . . *Instant start-up.* The System 500 is ready to start working almost as soon as it's out of the box. Send now for free brochure.

Nicolet Test Instruments Division

5225 Verona Road, Madison, WI 53711-4495, 608/273-5008 or 800/356-3090

Nicolet

INSTRUMENTS OF DISCOVERY

CIRCLE NO. 46

ICs provide full-duplex, synchronous communications via single optical cable

If you've been looking for a way to significantly reduce the expense of fiber-optic communications, the CS8123 and CS8124 Optimodem monolithic ICs provide full-duplex synchronous transmissions over a single, 1300m optical cable. By implementing a digital calibration scheme to control the bandwidth of the linear channel, the CS8123 and CS8124 become so sensitive that you can use a simple LED as a detector.

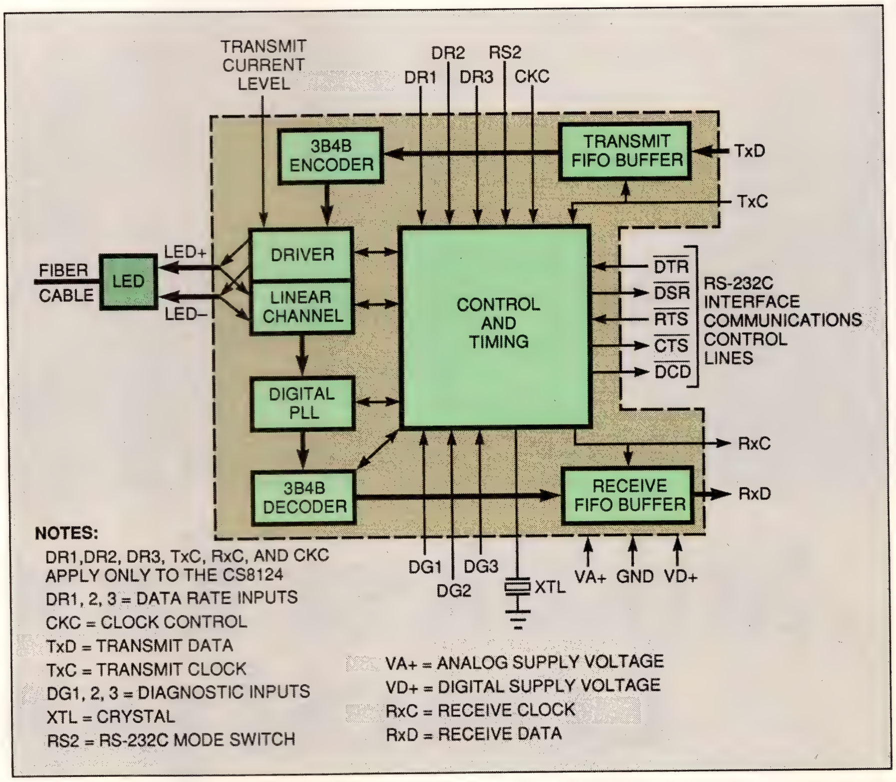
This level of sensitivity also permits you to use inexpensive plastic cable that can cut your system's cabling costs by 30%. Furthermore, you only need $40 worth of components to create each chip-based termination, compared with the current $150 per end you'd have to pay for lower-function, asynchronous modules.

The chips send and receive serial binary data by encoding, decoding, and buffering data to implement a time-compressed and multiplexed "ping-pong" channel. Synchronization logic continually switches each device and its respective LED from transmit mode to receive mode, thus creating a bidirectional "ping-pong" communication. If you choose to use a higher data rate on the optical cable than is necessary for end-user applications, you'll find that a half-duplex ping-pong link can support a full-duplex end-user connection.

Four optional secondary-control channels provide 1-kHz independent end-to-end transmissions that can operate in parallel with the primary communications link—an especially useful feature for transmitting RS-232C control data. In addition, the CS8124 gives your system synchronous communication at 2.4k, 9.6k, 19.2k, 64k, 160k, 192k, and 256k bps. Both chips offer full-duplex asynchronous operation to 38.4k bps. You can provide external transmit clocks for each link, or the chips can internally generate a clock cycle. And flexible clocking modes allow you to establish asynchronous transmit clocks at each end of a single link.

An internal master clock operates in each chip at one-sixth the frequency of your circuit's oscillator. A machine cycle of 128 master-clock cycles provides four periods: time to transmit; a delay period; time to receive; and another delay period. Each chip establishes the length of the delay periods to adjust the position of the transmit window and the receive window to provide signal-propagation time along the length of the cable.

A digital phase-locked loop performs timing recovery to maintain synchronization between the master and slave chips. An internal jitter attenuator reduces clock jitter



***This Optimodem IC provides bidirectional communications over a single fiber-optic cable** by using synchronization logic that establishes an alternating "ping-pong" type of communication link. The chip includes RS-232C handshake lines to reduce external circuitry.*

Smallest footprint. Lowest power.

A Spanking-new Family of 5-Volt Devices for Power-stingy Disk Drives.

If you're designing disk drives for use in applications where low power and small footprint are important, you need Silicon Systems' new family of low-power read-channel devices.

The family consists of three 5-volt-only high performance read-channel devices – the SSI 32R1200, SSI 32R4610, and SSI 32P548. The 32R1200 (Ferrite/MIG) and the 32R4610 (Thin Film) are R/W amplifiers – each providing a low-noise read amplifier, write drivers, and data protection circuitry. The 32P548 (Pulse Detector/Data Synchronizer) is a highly integrated combination circuit containing complete pulse detection, data synchronization, and embedded servo capture electronics.

An entire data channel using this 5-volt family is capable of operating on a stingy 750mW while still providing high performance. Alternate design solutions often consume as much as two to three times more power. In addition to low operating power, two independent power-down states are provided. The first is a sleep state included in each device for power savings during idle conditions. The second state, contained in the 32P548, powers down circuitry not required during servo acquisition.

The 32P548 comes in a 52-pin fine-pitch quad flat pack (body 390 x 390 mils) and the 32R1200, 32R4610 Read/Write devices are available in standard 16-pin and 20-pin SO packages.

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Circle 126 for Product Information

EDN EDITORS' CHOICE

that may result from the ping-pong operation and line-code decoding. And a calibration circuit tunes the bandwidth of the chip's amplifier to prevent high-frequency noise from getting into the chip.

You can use chip links with a terminal concentrator to connect several computer terminals to an FDDI (Fiber Data Distribution Interface) network at a low cost. Another application lets you reduce the cable and connector congestion of RS-232C matrix terminations by substituting optical cables in high-capacity data PBXs and matrix switches. When weight is a consideration, optical cables offer an advantage over heavier copper wire. In addition, the chips can transmit data more than 1000m at 256k bps, whereas RS-232C cables are limited to 100m transmissions at 19.2k bps. Optical communications also provide secure voice and data communications, superior electrical noise immunity, and minimal risk of electrical sparks in explosive atmospheres.

Currently available in production quantities, the CS8123 sells for \$17.70, and the CS8124 costs \$21.30 (100).—***J D Mosley***

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222. FAX (512) 445- 7581.

Circle No. 733

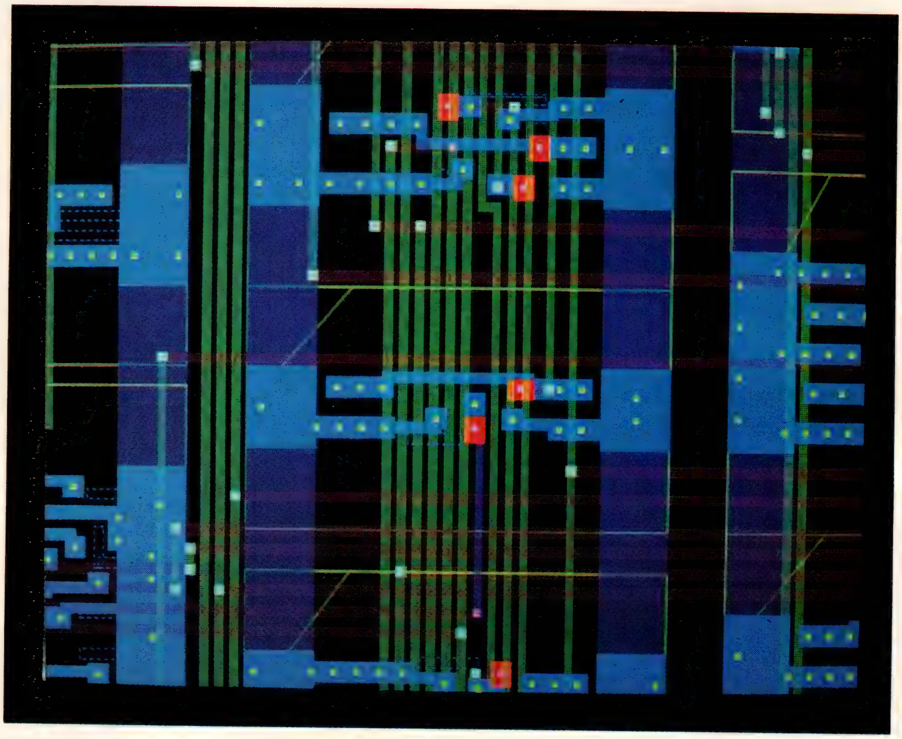
3-layer-metal, IC layout software increases circuit density

Routing channels on an IC are a consequence of your need for places to run interconnect. These channels are space hogs that typically occupy over 50% of the total chip area. Cell3 Ensemble is a 3-layer-metal, IC place-and-route layout tool for mixed blocks and standard cells that, coupled with a 3-layer-metal fabrication process, could eliminate many of the routing channels.

The software, integrated within the vendor's design framework, disposes of routing channels via a generalized cell model and an obstruction-based routing algorithm that allows over-the-cell routing. You can, however, guide the software using megacells placed as hard- and soft-macro cells. The software also allows iterative improvements.

The benefits of 3-layer-metal routing are significant. First, over-the-cell routing minimizes the routing channels and improves circuit density. Second, circuit performance improves because of the shorter lengths and lower capacitance seen by the interconnect. Finally, as a result of the density improvements, the number of die per wafer increases, thus balancing the increased processing cost of the more complex 3-layer-metal technology.

To minimize the risk of timing problems creeping into your design as you lay out the IC, the vendor offers two options to the Cell3 Ensemble. A timing-assurance capability utilizes the design framework to integrate static timing analyzers and logic simulators into the layout exercise. This capability lets you specify system delay constraints for critical paths. The timing-assurance tool also incorporates parameter extraction to accurately model circuit delays.



***With three layers of metal for routing**—blue is metal 1, red is metal 2, and green is metal 3—Cell3 Ensemble lets signals go over cells to their destination.*

The second option to the layout software is clock-tree synthesis. This option uses a clustering algorithm and balanced-tree routing to partition the clock nets. The result is balanced signal loading via a properly buffered clock that minimizes skew.

Cell3 Ensemble and the timing-assurance and clock-synthesis options are available on Apollo/HP 3500, 4500, and 10,000 workstations; DEC VAX 8500, 8600, 8700, and 8800 VMS mainframes; Intergraph 200 and 300 workstations; IBM VM/XA mainframes; and Sun 4 and SPARCstation workstations. Depending on what hardware you're running, licenses start at $100,000 for the Cell3 Ensemble. The timing-assurance option costs $36,000 and the clock-tree synthesizer costs $28,000.

—Michael C Markowitz

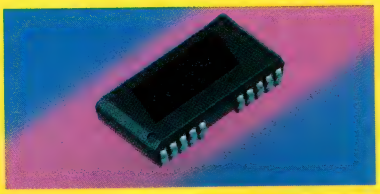
Cadence Design Systems, 555 River Oaks Pkwy, San Jose, CA 95134. Phone (408) 943-1234.

Circle No. 730

UESS, WHO'S ONCE AGAIN: TIMES BETTER.

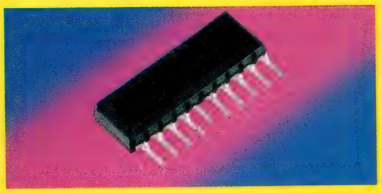
4 MDRAM

Now, in 1990, we're out to make it happen again: To reach the next technological peak, first. Offering our customers mass-produced 4 MBit DRAMs. To give you an idea: by March 1990, our monthly output of 4 MBit DRAMs will break the one million barrier.



1 MDRAM

In 1985, we were the first to go into full-scale production of the 1 MBit DRAM. Since then we've led the market for these super components.



Any guesses who's now pulling off this staggering mega-double? And whom you should call a.s.a.p. for the latest information on the new 4 MBit DRAM? Turn over and find out.

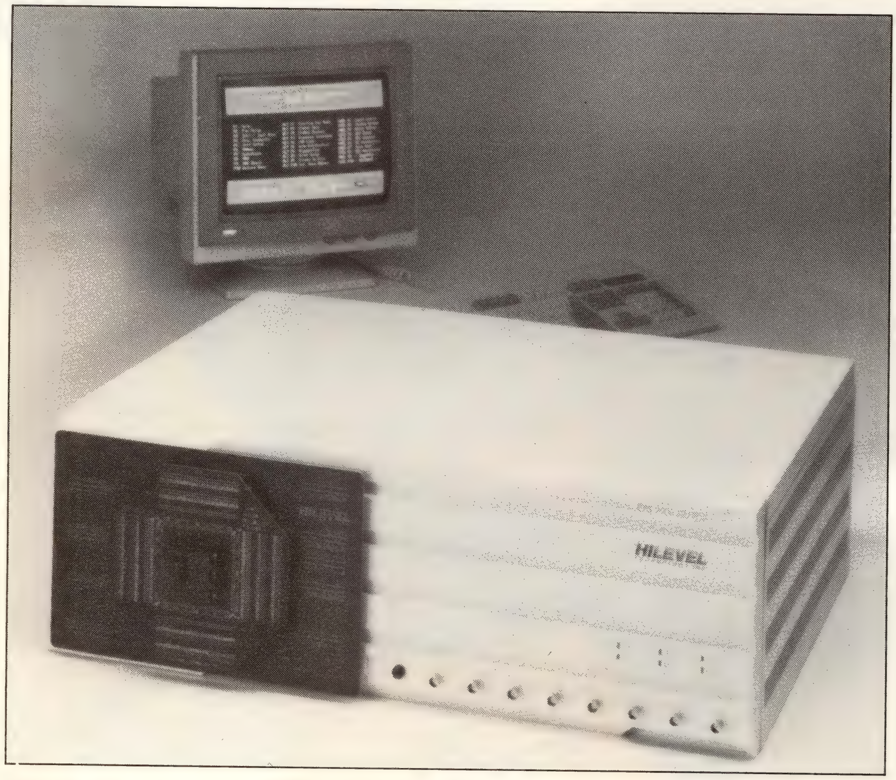
CIRCLE NO. 48

ASIC tester costs less than $1000/pin, operates at 100 MHz, and can vary loads

At less than $1000/pin, the ETS 7000 makes ASIC testing and verifying affordable for small companies and engineering departments. Furthermore, this new benchtop tester offers features such as variable slew rate and programmable loads. The device operates at speeds as high as 100 MHz and, therefore, can test most ICs at full operating speeds.

The ETS 7000 occupies 9×27×22 in. on a bench and weighs 125 lbs. A separate control unit, actually an 80386-based PC in a tower configuration, rests on the floor. The system can accommodate eight 16-pin test modules for a maximum configuration of 128 pins.

The tester's slew rate is variable from 0.2 to 1.5V/nsec, which simplifies testing of mixed technology devices such as BiCMOS. The variable-slew-rate capability also allows you to test devices fabricated with most old or new technologies.



The variable slew rates *and 100-MHz test rate of the ETS 7000 allow you to test ICs fabricated with a variety of technologies, including mixed technologies such as BiCMOS.*

You can program the tester on a pin-by-pin basis; the system guarantees a worst-case pin-to-pin skew of ±500 psecs. By setting all pins for split-cycle I/O operation, you can test features such as multiplexed bidirectional buses in µPs. You can also program loads on selected pins to completely characterize a device. Both input receivers and output drivers offer ranges programmable from −2 to +6.5V. Sixteen timing generators can be assigned to pins; timing resolution is 100 psec.

The tester performs scan testing compatible with IEEE P1149.1. A pattern generator allows you to set up sequential tests. The tester can produce a 2-axis shmoo plot based on any two variables; for example, voltage and time. You can also customize the way the tester displays and highlights acquired vectors.

A 128-pin system offers storage for 601k vectors/pin, and a 32-pin configuration will allow you to store as many as 1.8M vectors/pin. The tester automatically calibrates all voltages, timing, and skew parameters. You can perform automatic calibration with the device adapter connected to the tester via a cable. Therefore, you can test and characterize devices in environmental chambers.

The basic system costs $934/pin and includes the tester chassis, the computer/system controller, and IBM VGA color graphics. Field-upgradeable options for the ETS 7000 include additional 16-pin modules (to the maximum 128 pins), a variable-slew-rate software utility, a parametric measuring unit, and an adaptive software package for developing C programs for custom testing. The tester is available now with delivery 60 days ARO.

—Maury Wright

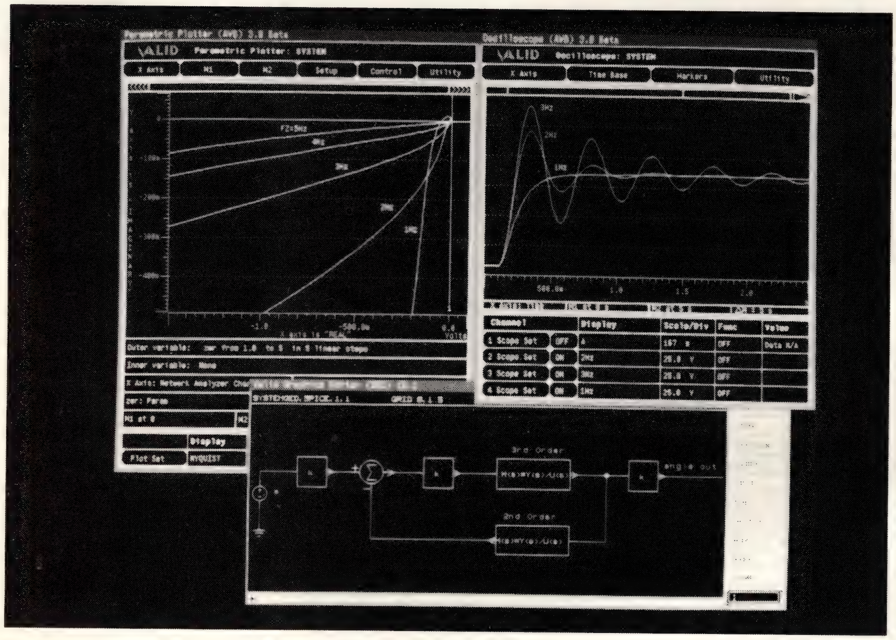
HiLevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (714) 727-2100. FAX (714) 727-2101.

Circle No. 731

Software package integrates analog design, simulation, and layout

The heart of the Analog Workbench II software package is a communications manager that provides communications between all design and analysis tools in the software package as well as third-party tools. These simulation tools also work with the vendor's schematic-capture and layout tools.

For device-level simulation, the software package uses Spice Plus, a modified version of Spice 3. An optional library provides more than 4300 models. You can also run behavioral simulations, using functional blocks from a library of more than 100 functions. The Function Block Library lets you create behavioral descriptions with a graphical, menu-driven set of mathematical constructs.



You can design at the behavioral, functional, or circuit level, *then simulate with the Analog Workbench II software package. The package lets you run 10 Spice simulations simultaneously on 10 workstations in about one-ninth the time it would take to run all 10 simulations on one workstation.*

To speed up circuit simulation, the software package has a network-distributed-processing option that lets you run simultaneous Spice Plus simulations on multiple workstations. You can use this option when you want to run a simulation with multiple parameter values such as a sensitivity check to see which parameter value results in the best circuit performance.

When using the distributed-processing option, each workstation runs a separate Spice Plus simulation. The software uses the network only to initialize the simulation and return the results, keeping the communications overhead low. The manufacturer claims network-distributed processing is about 90% efficient. For example, if you run 10 Spice simulations simultaneously on 10 workstations, the operation would take about one-ninth the time it would to make all 10 runs on one workstation. The network-distributed-processing capability is also a time-saver for Monte Carlo analysis.

Using behavioral simulation, you can make an initial simulation and use high-level function blocks to test out your system design before figuring out how to implement the simulation in a schematic. Once you're convinced your plan will work, you can replace function blocks with the schematic design. You can mix function blocks and Spice Plus models in the same simulation.

Furthermore, the software package provides a checkpoint restart capability that lets you stop a simulation at a predefined point and restart from the same point. You can set checkpoints at regular intervals to protect against a system crash or accidental interruption during long simulation runs.

You can also use the checkpoint restart to shorten simulation times by modifying component values and simulation parameters at a checkpoint and restarting the simulation. Restarting at a checkpoint avoids the need to rerun the simulation.

The software package runs on Sun, DEC, HP-Apollo, and the IBM RT. The base price of Analog Workbench II, which includes the Communications Manager, basic analysis tools, and the Spice Plus simulator, starts at $10,000. The Function Block Library sells for $5000. Analog Workbench II is free to participants in Valid's software-support program and for installations still under 90-day warranty.

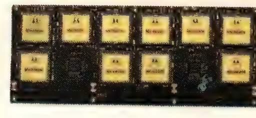
—Doug Conner

Valid Logic Systems, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 432-9400. FAX (408) 432-9430.

Circle No. 732

READY-TO-WEAR RISC, FROM MOTOROLA.

X-SMALL.



RISC HYPERmodules.™ A
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Plug-in daughter-cards a
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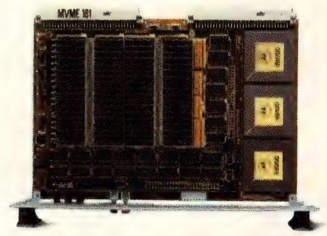

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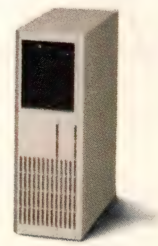

RISC Entry-Level Compu
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RISC Mid-Range Compute
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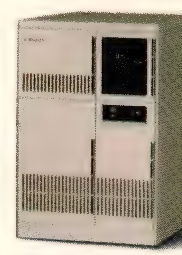

ACCESSORIES

In RISC, one size does not fit all. But one family of products does: Motorola's.

We give you a complete selection of ready-made RISC choices: from microprocessors to VMEmodules to integrated systems—all with standard software and networking capabilities. Plus we can tailor a solution that's just right for your system build through Application-Specific Computing.™

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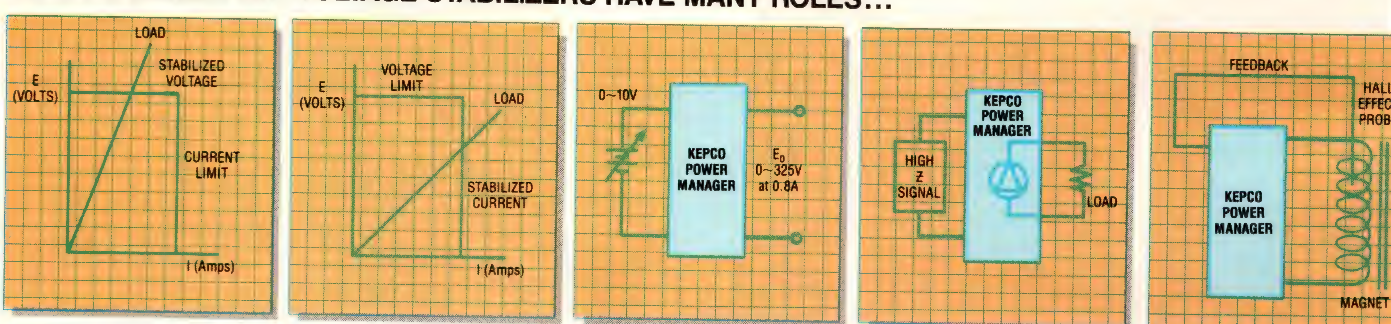
Multi Roles. One actor, many faces...

One power supply, many applications.

KEPCO'S SERIES ATE VOLTAGE STABILIZERS HAVE MANY ROLES...



....SUPPLY STABILIZED VOLTAGE
0.001% voltage stabilizer

AND CURRENT.
0.005% current stabilizer

THEY'RE PROGRAMMABLE IN VOLTAGE MODE.
A voltage stabilizer controlled by a 0-10V d-c signal

THEY'RE PROGRAMMABLE IN CURRENT MODE.
A current stabilizer controlled by a high impedance source

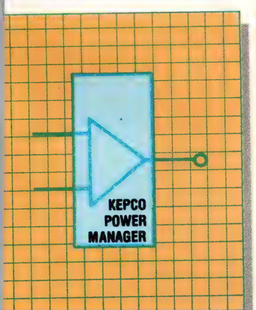
THEY'LL ACCEPT FEEDBACK.
A magnetic field stabilizer controlled by a Hall-effect senso

Model ATE 325-0.8M

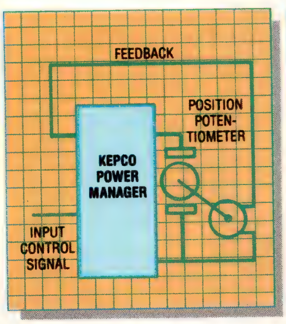
The actor/model is *Jan Leighton*, whose face has been photographed as everyone from Patton to MacArthur to Lincoln. One face, many roles. More than 3,372 historical notables according to his fact sheet!

The power supply is Kepco's ATE. While it cannot claim quite so many roles as Jan Leighton, its flexibility will delight you. ATE power supplies are comfortable in roles as voltage sources, current stabilizers, power amplifiers, GPIB listeners and MATE-verified talker-listeners.

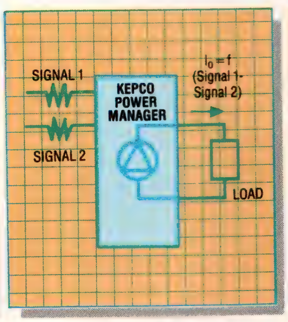
ATE are comfortable on your bench, in your systems or installed in your test rack ... you can control them with analog signals or digital. You can use their integral uncommitted op amps to scale, sum, integrate or multiply a variety of signal stimuli in servo roles. A versatile piece of test equipment indeed.



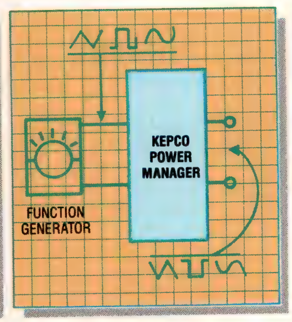
THEY'LL FUNCTION AS AN AMPLIFIER...
A self-powered oversized op-amp



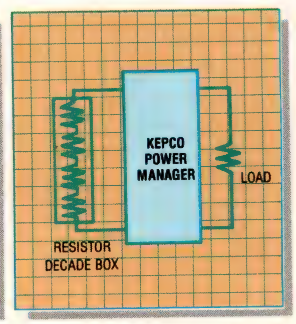
OR CONTROL A MACHINE.
A servo amplifier to drive a positioning motor



ATE CAN SUM INPUT CONTROL SIGNALS
A current stabilizer controlled by the difference between two signals



...BE DRIVEN BY AN ANALOG FUNCTION
A voltage stabilizer controlled by a signal generator



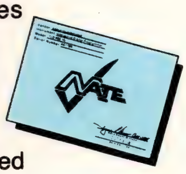
OR INTERFACE TO THE DIGITAL WORLD
A voltage stabilizer controlled by a passive resistance decade box

ATE are made in 5 power ranges, 50 to 1000W (voltage ranges 0-6V to 0-325V) to afford:

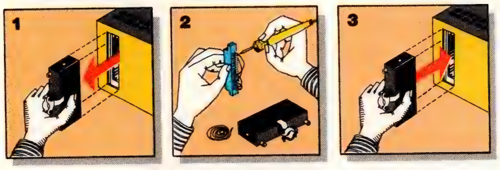
- ☐ High stability (less than 0.0005% source effect, 0.001% load effect).
- ☐ Very low ripple and noise (0.1mV rms, 1mV pp).
- ☐ Rapid recovery (<50µsec).

Most important... ATE's linear design supports a fast-programming mode which — for your control signals — allows a wide bandwidth response ... 16KHz in our 0-6V, 100 Ampere model, allowing roles ordinary power supplies cannot imagine.

- ☐ *Fast Recovery* current stabilizer
- ☐ *Wide band* power amplifier
- ☐ *Rapid response* to sequenced programs



Like Jan Leighton, Kepco's 41 different ATE models are capable of many roles, limited mainly by your imagination. We'd like to tell you more. Please write or call and request Kepco's new 1990 edition Catalog and Handbook (146-1678).



ATE's unique user port allows you access to the principal control points. A simple 3-step procedure allows you to configure your ATE for whatever role you require.

By appropriate wiring of the mating plug, your ATE easily assumes a variety of roles: voltage/current controller, resistance programmed, voltage programmed, digitally programmed, power amplifier, servo amplifier, integrator.

SEE US AT ELECTRO/90 KEPCO BOOTH 3406, 3408.

For your free copy of Kepco's new 120-page Linear Power Supply Catalog (#146-1678), call/fax/write to Dept. LLT-12,
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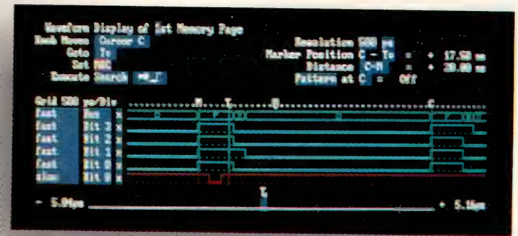
KEPCO®
THE POWER SUPPLIER™

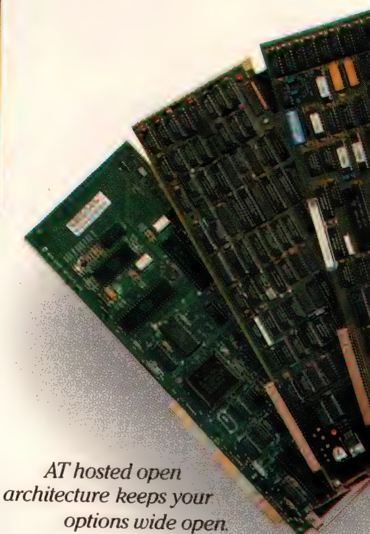
CIRCLE NO. 55

No matter what you high performance logic

Our Rotary Mouse™ gives you the easy, intuitive performance of a mouse with no mouse mess on your bench.



With 500 pS timing resolution, no variation is too subtle for detection.

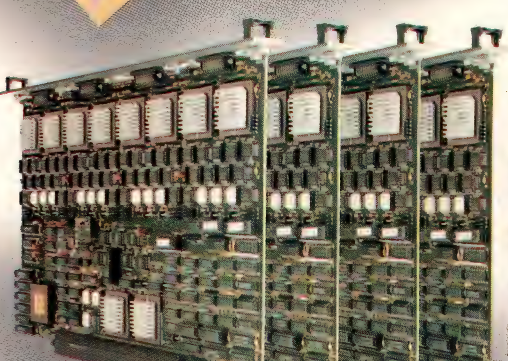


AT hosted open architecture keeps your options wide open.

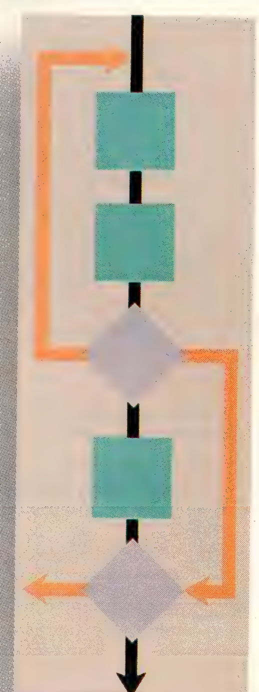
A clustered-channel bus display simplifies the timing diagram so you always know exactly where you are on multiple buses at a glance.

Advanced transitional recording techniques give you at least 5 times more recording time, with more high speed channels.

Even the most elusive signals can't escape VHSTA probes with 800 pS pulse capture.



All the channels you'll need at 100 MHz are in one mainframe. Configure them as up to 4 independent logic analyzers and disassemble up to 4 microprocessors at a time.



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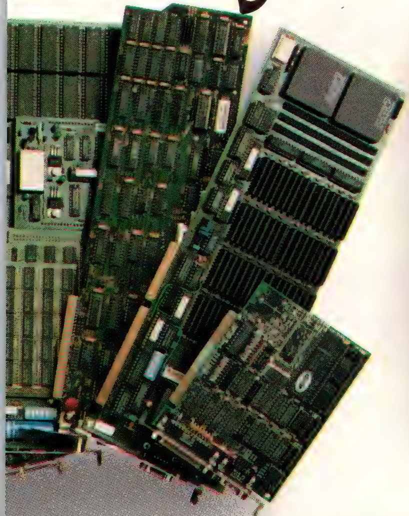

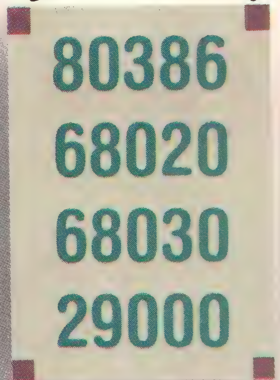

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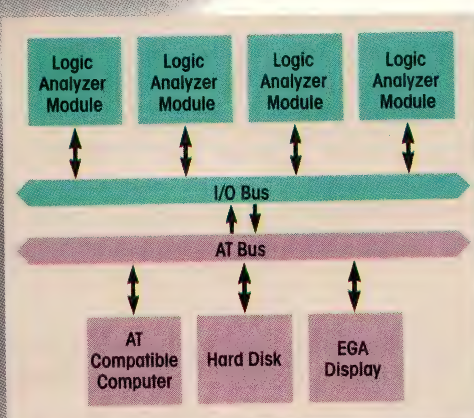

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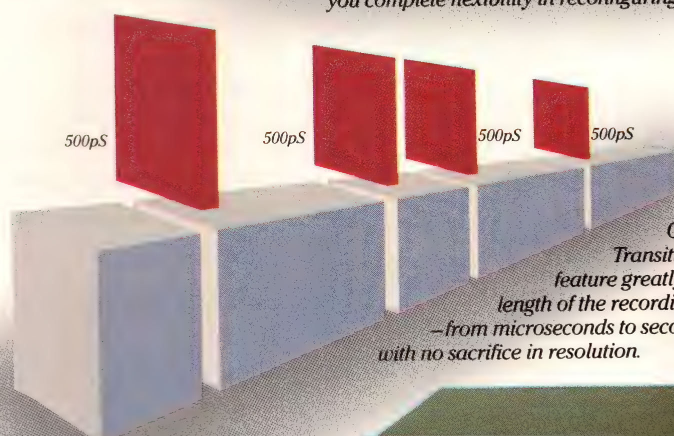

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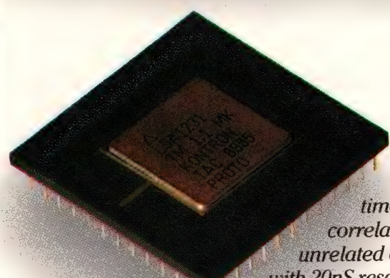

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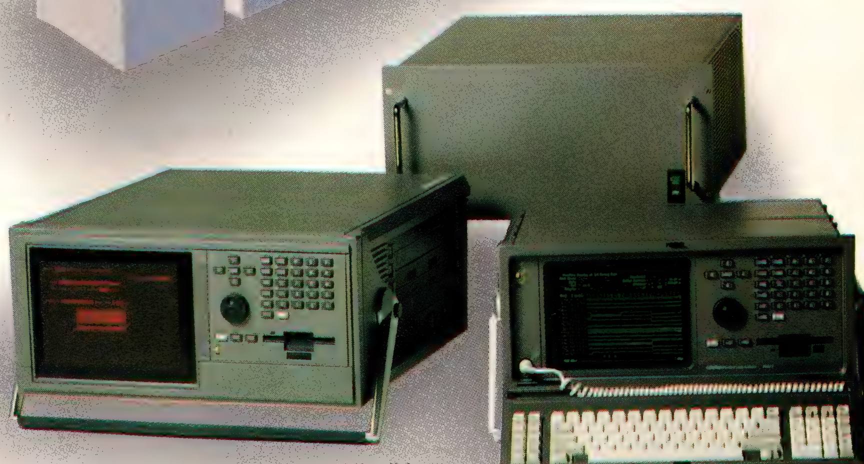

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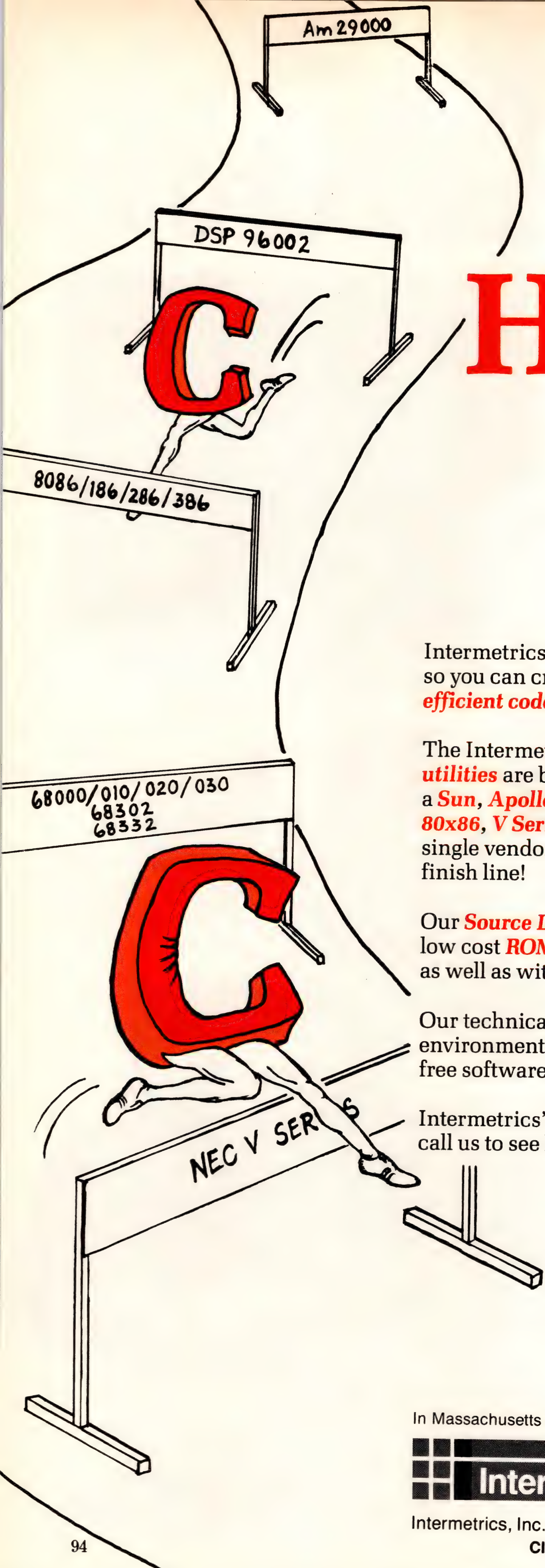

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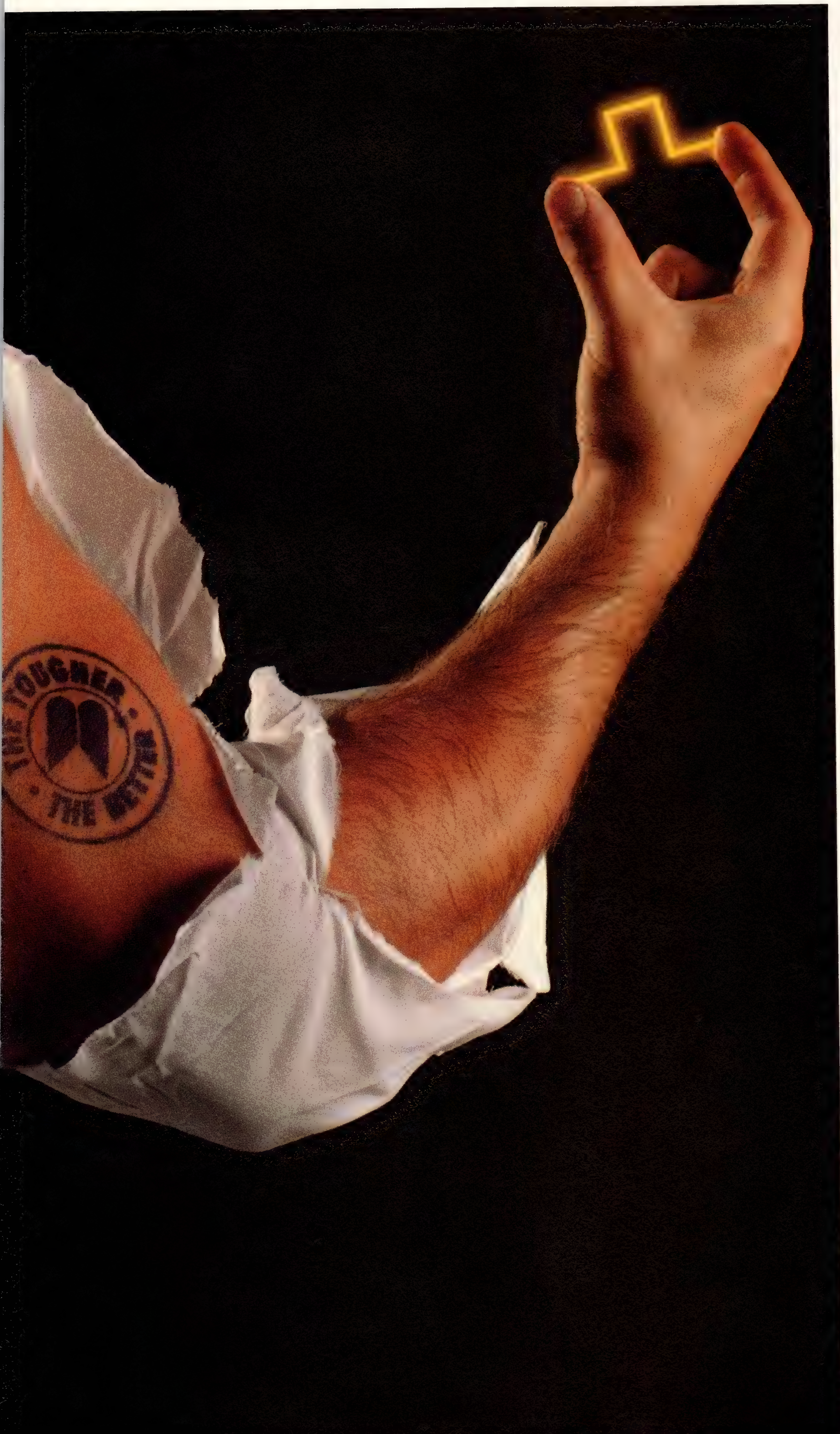

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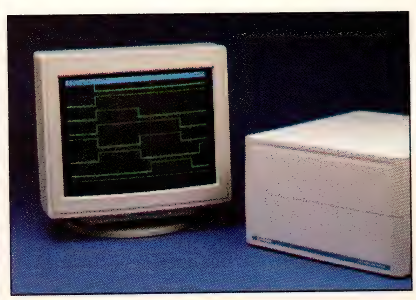

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C compilers for real-time software

If you're developing software for real-time systems, your C compiler should provide good interrupt-handling facilities, fast context switching, a clean assembly-language interface, selectable optimizations, and it should be able to handle a fragmented memory map.

Chris Terry, *Associate Editor*

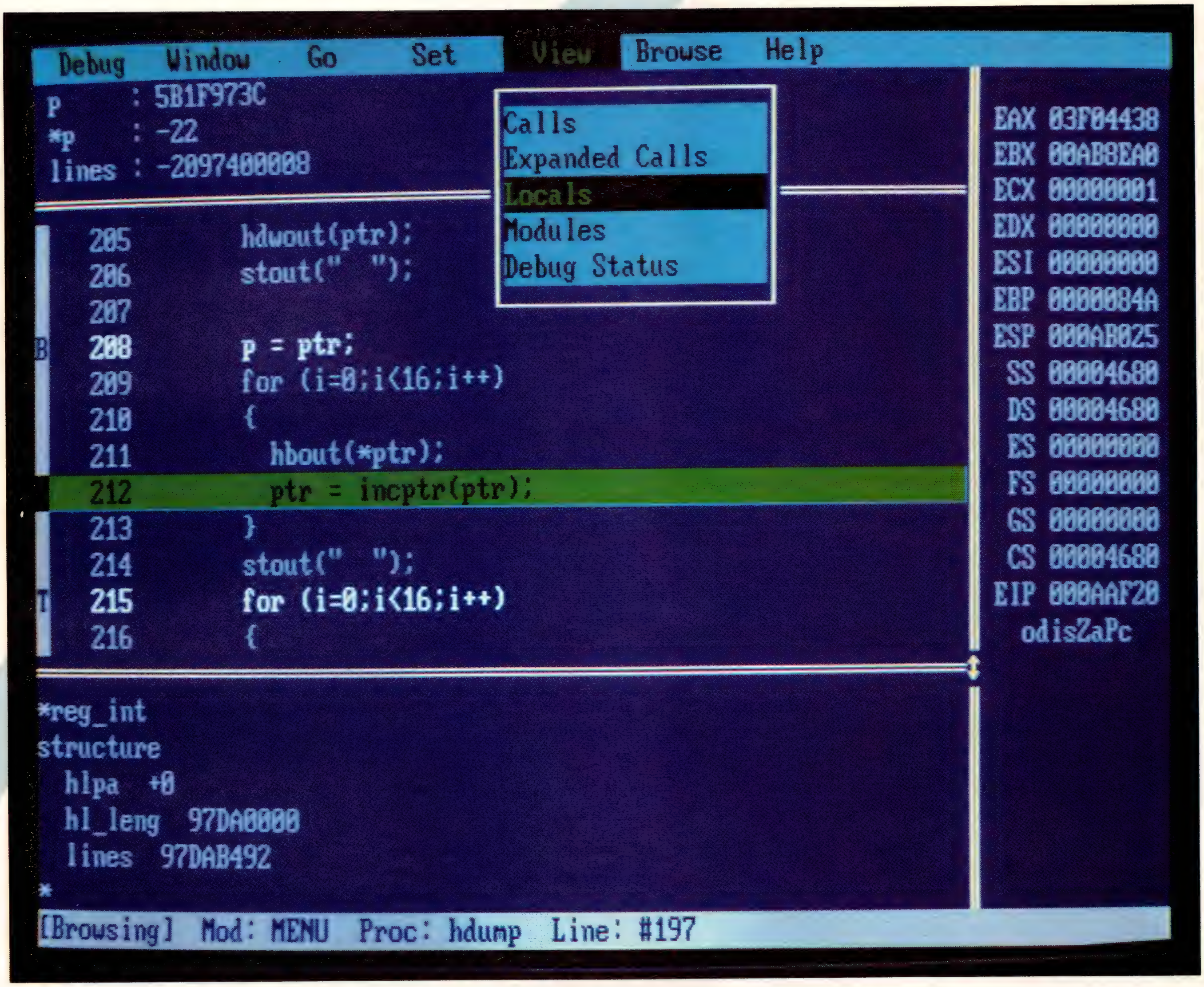
For years, it's been an engineering axiom that compilers can't generate code that's fast enough for real-time systems—assembly language is the only way to go. That viewpoint was once justifiable, but advances in optimization techniques and the increasing complexity of real-time systems are turning the axiom into a myth. The process is slow because, although the C technology is in place, it's not easy to convince an experienced assembly-language programmer that he should abandon his tried-and-true techniques in favor of a new language.

"Real-time" is a term that was once restricted to clock/calendar mechanisms. It distinguished the tracking and reporting of real-world dates and times from the measurement of accumulated CPU time (which formed the basis on which to charge a customer). Nowadays, the term refers to computer systems whose primary function is to interact with external sensors and control mechanisms in performing tasks that are interdependent and have stringent time constraints.

This definition is still fuzzy, however, because every computer system executes certain tasks that have such constraints. For example, you wouldn't describe a personal computer as a "real-time system" on the grounds that it has serial data ports and must read these in timely fashion or lose data. A PC may perform some real-time tasks, but it's basically a general-purpose machine that processes data contained in its own files.

"Real time" is an entirely appropriate label, however, for systems in which the sequence and duration of external events are of prime importance—for example, in an industrial process-control system that interacts with dozens of sensors and controls, or in a training simulator that receives data from the pilot's flight controls and must immediately change the physical attitude of the training vehicle and the view presented to the trainee.

An important part of writing code



The DB386 source-level debugger *from Intel lets you browse through particular types of variables and see the associated assembly-language code.*

that will execute quickly is choosing the best algorithms and then selecting coding techniques that eliminate unnecessary operations (**Refs 1, 2**). Most compilers perform some degree of optimization that will result in speedier execution. The two kinds of optimizations are global optimizations, which are essentially machine independent; and architecture-specific optimizations, which take maximum advantage of a CPU chip's hardware features. For real-time software design, you'll want a compiler that lets you turn the optimizations on or off, because some techniques may make assumptions that aren't valid in your system.

The most common global optimizations are common-subexpression elimination, constant unfolding, removal of dead code, loop unrolling, and strength reduction. Common-subexpression elimination aims at evaluating an expression only once, as long as the parameters don't change between uses of the expression. A typical example would be

$$a[i] = i + (j * k)$$

occurring within one or more loops, when $(j * k)$ can be computed outside the loop—or even outside the function.

Removal of dead code (code that never gets executed) reduces program size. You might think that a well-designed program would have no dead code; however, revisions to the code, or even the rearrangements produced by optimizations, can sometimes result in dead code that is difficult to detect using manual methods.

Loop unrolling consists of replac-

ing a loop by repetitions of in-line code; the in-line code executes much faster than the loop but is usually much larger. For that reason, certain compilers (such as the Intel C-386/i486) that are aimed at embedded systems don't use loop unrolling at all.

Strength reduction is a technique that's specific to C code; it consists of replacing certain types of multiplicative address computations with pointers to the required elements. The compiler will easily identify computations that multiply or divide by a power of two and generate the appropriate left or right SHIFT instruction instead of a MULT or DIV instruction.

Understandably, designers of real-time systems tend to be wary of automatic optimizations of these kinds, especially because the resulting assembly-language output is very difficult to unscramble. A source-level debugger is a necessity—not a luxury—for optimized code; some engineers believe that if you simplify matters by debugging unoptimized code, there's no guarantee that your code will remain bug free after optimization, especially if timing margins are very narrow.

ANSI conformance can help

Some of the older optimizing compilers can detect multiple reads (without intervening writes) at the same memory address and, assuming that the contents of that location have not changed, they eliminate all reads but the last one. This trick can cause havoc if the address corresponds to a memory-mapped I/O device. Fortunately, if your compiler conforms to the ANSI draft specification of C, you can specify the data as type *volatile*. Then, even if your compiler performs this kind of optimization, it won't try to eliminate multiple reads from a

Features of ANSI C, such as the const and volatile data types, allow C to meet real-time requirements.

memory-mapped peripheral. You should be aware, however, that because of the widely varying needs of developers, the ANSI committee didn't specify the precise behavior of the *const* and *volatile* data types. The implementation of these data types is left to the compiler vendor, who should document their behavior in sufficient detail for you to use them with confidence.

Several other ANSI extensions of the language, such as function prototypes, make the language more amenable to the needs of the designers of real-time systems. Almost all of the compilers that have appeared in the last year or two provide the ANSI extensions.

μP-specific optimizations

Because every compiler or cross-compiler serves a specific μP chip, it must have information about how the instructions of that chip operate. Thus, because the Motorola 680x0 family has many registers, a C compiler targeted for those chips will use as many *register* variables as possible. The allocation of variables to registers is also essential for the AM29000 and other RISC processors. Likewise, the 680x0 family has addressing modes that simplify access to subscripted arrays, and the optimizing features of the Intermetrics compilers take full advantage of these modes. These compilers are part of the Intertools tool sets, which run on a wide variety of host computers and target most common microprocessors and single-chip microcontrollers. For a PC host, prices for the cross-compiler start at $1000 (or $1800 including the cross-assembler); for Sun or Apollo workstations, the cross-compiler costs $2500.

Microtec Research is another company that offers ANSI C cross-compilers for the 680x0 family, as well as its cross-assembler and the Xray debugger. These tools run on PCs, Sun and Apollo workstations, and Vax computers. Prices for a C development system start at $2800. The compiler performs both global and architecture-specific optimizations. You can turn optimization on or off and optimize the code for either maximum speed or minimum space.

Introl Corp offers C cross-compilers and debuggers targeted for the National Semiconductor 32000 μPs as well as for the Motorola 680x and 680x0 families. Macintosh-hosted versions cost $2000 for the cross-compiler and $1000 for the debugger; versions are available for host computers ranging from the IBM PCs through Sun and Apollo workstations to the HP9000 and DEC Vax Series; prices depend on the host.

A recent trend seems to be for vendors of real-time kernels and development tools to bundle C compilers from companies that specialize in compilers. Ready Systems, for example, includes the Green Hills cross-compiler from Oasys (Waltham, MA) in the VRTX Velocity development system for 680x0 systems. Versions are available for Force Computers' CPU-30 VME board and the TSVME-133 board from Themis Computers, both of which are based on the 68030. Prices for VRTX Velocity start at $19,970.

A similar relationship exists between BSO Inc (Boston Systems Office) and Tasking BV of the Netherlands, which have formed an alli-

ance and are now supplying a series of BSO/Tasking cross-compilers that run on DECstation 2100 and 3100 RISC-based workstations. The initial offerings consist of both PL/M and C cross-compilers for the 8051 microcontroller, and C cross-compilers for Motorola's 68000 and 68020 µPs and Intel's 8096 and 80196 microcontrollers. Prices start at $4500 for the DECstation 2100 host. BSO also offers an extensive range of its own cross-development tools for DEC hosts.

Using C for DSP software

In the DSP world, new hardware features are appearing. For example, the Motorola DSP96002 chip has two memory spaces, designated X and Y, and hardware that eliminates much of the overhead associated with software loops. The optimizer of the Intermetrics compiler makes extensive use of the loop hardware, and by rearranging the code and coalescing instructions, the optimizer can make the CPU access the X and Y memories simultaneously instead of sequentially.

In its 2100 fixed-point DSP chip, Analog Devices includes architectural features that make it easier to optimize programs written in C, and the company offers an optimizing compiler to support the chip. Prices start at $1500 for a PC-hosted version.

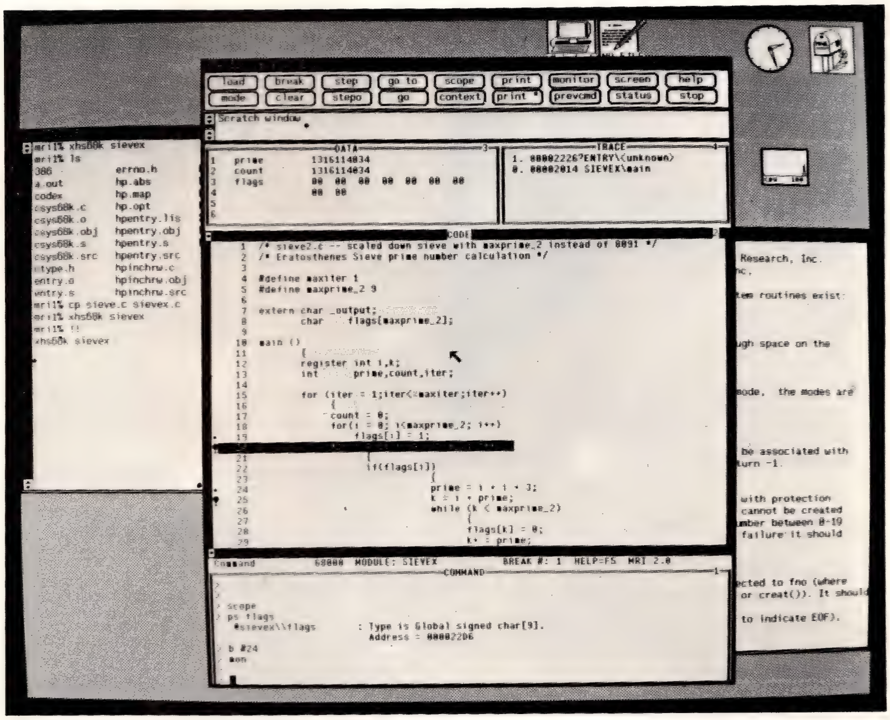
Texas Instruments also offers both an optimizing ANSI C compiler and a source-level debugger for its 320C30 DSP chip. The optimizations include register variables, parallel instructions, delayed branches, jump optimization, and loop rotation. Compiler prices start at $2500 for the PC and Macintosh versions.

Intel's C-386/486 compiler has features that can eliminate much of the overhead in real-time systems. For example, compiler directives can give you good control of bit fields and let you include in-line assembly-language code. Other directives give you control of segmentation and let you build *subsystems* that may consist of several code modules. A system of "near" and "far" references lets you work easily with these subsystems. Normally, you'd use near references for calls to functions within the same subsystem and far references for calls to functions in other subsystems or at a different level of protection.

Many single-chip microcontrollers also have architectural features that require special handling by the compiler. For example, the 8048 and 8051 both have separate address spaces for code and data, and the stack space is extremely limited.

When you're designing a system that will interact with multiple, asynchronous I/O devices, good interrupt-management facilities are a necessity. Even though the C language gives you access to many of the low-level features of the CPU, the original Kernighan and Ritchie specification contained no built-in facilities for interrupt management.

Some modern C compilers, especially those designed for systems based on Motorola 680x0 or Intel 80x86 CPUs, have remedied this deficiency. For example, the Intel C-386/i486 compiler has an interrupt directive that defines a function as an interrupt function and makes it much easier to prioritize interrupts and to handle nested interrupts smoothly.



The Xray source-level debugger *from Microtec Research shows you both C source code and the resulting 680x0 assembly language.*

Essential library characteristics

For effective real-time design, the functions included in the run-time library *must* be both ROMable and re-entrant. You should also have full source code for the run-time routines—or at least for those you expect to use—because you may need to tweak them to resolve

timing conflicts. Further, because your target system will probably run under a kernel rather than under a full operating system, make sure that the kernel documentation includes templates in source code for the startup routines and detailed instructions on how to use them. EDN

References

1. Gilmour, Peter S, "Speed the execution of your µP/µC software," *EDN*, May 25, 1989, pg 177.
2. Gilmour, Peter S, "Tailor your code for limited memory space," *EDN*, June 8, 1989, pg 165.
3. Silverthorn, Lee, "Rate-monotonic scheduling ensures tasks meet deadlines," *EDN*, October 26, 1989, pg 190.

Article Interest Quotient
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Manufacturers of C compilers

For more information on C compilers such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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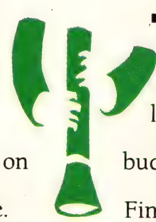

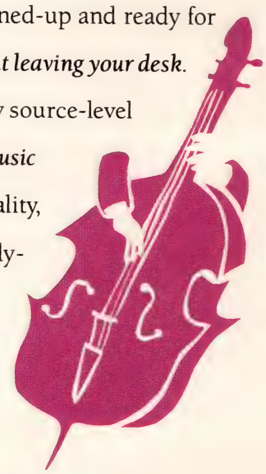

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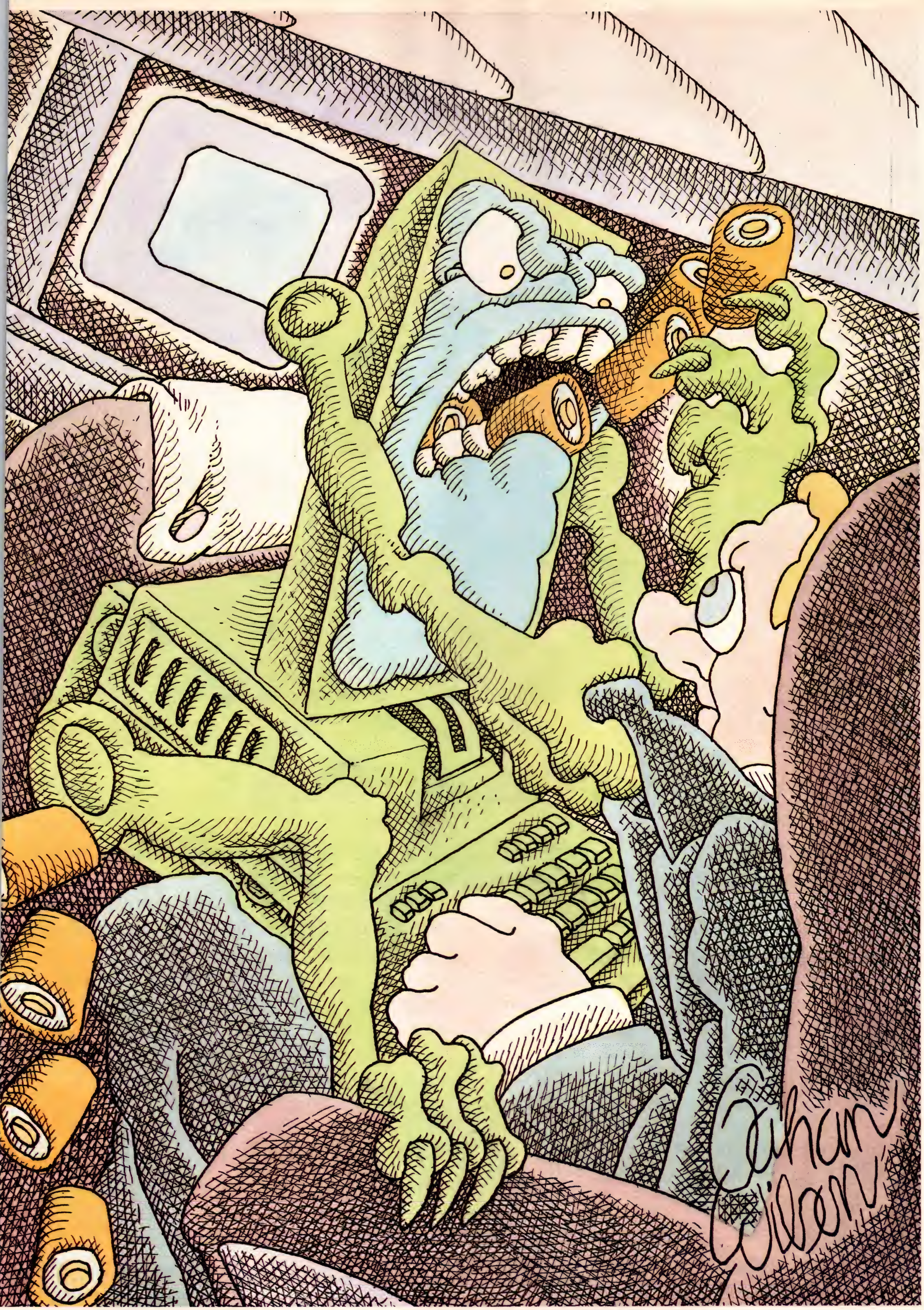
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MASS STORAGE

EDN's All-Star PC incorporates several mass-storage devices that provide flexible information storage and easy data interchange among PCs. We frequently crossed the thin line between the leading and the bleeding edges of data-storage technology as we tested various storage devices, host adapters, and peripheral controllers. What we learned applies to all types of computer systems, not just PCs.

IBM's original Model 5151 PC provided data storage on single-sided, 160k-byte floppy disks and on audio cassette tapes. The floppy-disk-drive capacity was mediocre, even by early 1980s standards, and the 200 bytes/sec audio-cassette interface was a joke. Fortunately, mass-storage capacity on PCs has come a long way since those humble beginnings. Floppy disks now hold megabytes of data, PC-compatible hard disks store hundreds and even thousands of megabytes, and tape drives store gigabytes.

EDN's All-Star PC incorporates eight mass-storage peripheral devices managed by three controller or host-adapter cards (**Fig 1**). Each of these three mass-storage subsystems—floppy disk, SCSI, and WORM (write-once, read-many) optical drive—has unique capabilities. The floppy-disk subsystem supports four floppy-disk drives, which furnish convenient, removable data storage and permit standardized

STEVEN H LEIBSON,
Senior Regional Editor

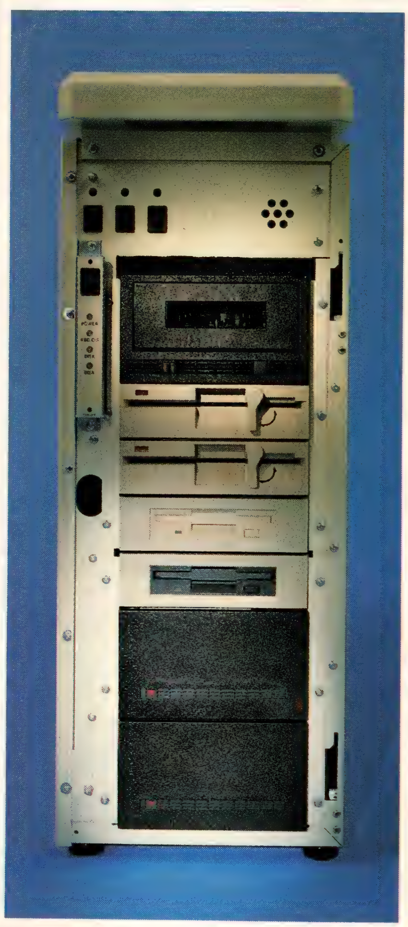
data interchange with other PCs. The SCSI subsystem controls two 330M-byte hard disks for the computer's primary data-storage needs and a 2.5G-byte tape unit for archival and backup storage (**Fig 2**). Finally, the PC's optical WORM drive provides indelible file storage on 1G-byte cartridges.

Floppy-disk drives are the one common element in every PC's mass-storage repertoire. IBM's floppy formats swept away the microcomputer industry's hundreds of 5¼-in. floppy-disk formats developed for the CP/M operating system. However, even IBM's 160k-byte disk format didn't last long. Microsoft's DOS 1.1 introduced a 320k-byte, double-sided format. DOS 2.0 added hierarchical file structures to the disk, bumped the single-sided floppy-disk capacity to 180k bytes, and increased the double-sided format's capacity to 360k bytes. The 360k-byte format's rapid proliferation consigned the earlier PC floppy formats to oblivion.

The next major change in PC floppy-disk formats occurred when IBM introduced its PC/AT with 1.2M-byte, "high-density," 5¼-in. floppy-disk drives. Then came 3½-in. floppy-disk drives that stored 720k bytes, followed by the introduction of IBM's PS/2 computers and 1.44M-byte, 3½-in. drives. Over a 9-year span, the PC, which had unified the industry's floppy-disk formats, evolved its own collection of incompatible formats.

The All-Star PC needed to accommodate these various floppy formats for maximum compatibility with other PCs. It needed at least two floppy-disk drives: a 5¼-in., 1.2M-byte drive and a 3½-in., 1.44M-byte drive. However, with only one 5¼-in. and one 3½-in. floppy-disk drive, the All-Star PC would not be able to duplicate floppy disks directly; it would have to temporarily store the information being copied on a hard disk while the source and destination disks were swapped in the floppy-disk drive. Because of an idiosyncratic aversion to 2-step floppy duplication, I decided early on that the All-Star PC would incorporate four floppy-disk drives: two 5¼-in. and two 3½-in. drives.

Meeting that 4-drive requirement was tough because most PC floppy-disk controllers manage only two floppy-disk drives. The All-Star PC would require a floppy-disk controller card that could manage four floppy-disk drives and support the PC's floppy-disk formats. The Compaticard IV from MicroSolutions Computer Products met these requirements.



Seven mass-storage peripherals cram the All-Star PC's 10 half-height drive bays. From top to bottom, the peripherals include a 2.5G-byte tape drive, two 5.25-in. and two 3.5-in. floppy-disk drives, and two 330M-byte hard-disk drives.

Table 1 lists the PC floppy-disk formats that the Compaticard IV supports. The Compaticard IV, along with one 5¼-in. high-capacity drive and one 3½-in. high-capacity drive, can read any standard PC floppy-disk format. The Compaticard IV also supports other types of floppy-disk drives, such as the now archaic 8-in. units, and can store 2.8M bytes on certain 3½-in. drives that accept a new type of floppy disk based on barium-ferrite media. The All-Star PC incorporates a 2.8M-byte floppy drive—an FD-235J from Teac America Inc. This drive can read and write standard 720k- and 1.44M-byte PC disks and can also use barium-ferrite disks. The All-Star PC incorporates three other floppy-disk drives from Teac—two FD-55GFR 5¼-in., high-density drives and one FD-235HF 3½-in. drive. Thus, the All-Star PC's full complement of drives includes two 5¼-in. and two 3½-in. units.

Twisted cables make it tough

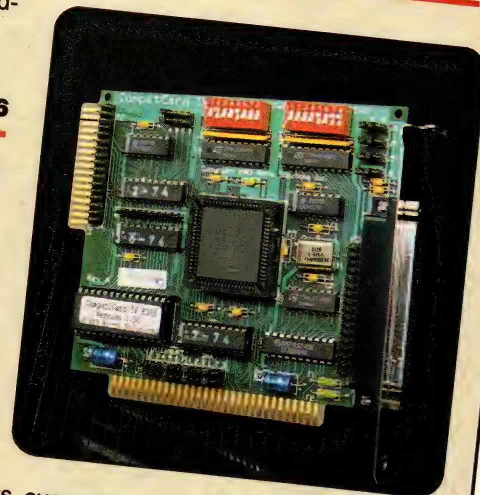
Two factors in IBM's floppy-disk-subsystem design complicated efforts to put four floppy-disk drives in the All-Star PC. The first is a very peculiar floppy-disk-drive cable for the PC. The cable includes a twist that interchanges the drive-select and motor-enable signal lines between the cable's two drive connectors. This cute scheme simplifies

EDN's PC All-Stars

Compaticard IV

MicroSolutions Computer Products, 132 W Lincoln Hwy, DeKalb, IL 60115. (815) 756-3411. FAX (815) 756-2928.

Circle No. 666



STATS:
BUS: PC or PC/AT
DRIVES SUPPORTED: 4
DRIVE SIZES SUPPORTED: 3½, 5¼, 8 in.
TRANSFER RATES: 1M, 500k, 300k, 250k bps
SPECIAL FEATURES: Boot from any drive, background formatting

BIO: The Compaticard IV supports every floppy-disk format ever created for the PC, and a few more. It can replace or work in tandem with a PC's existing floppy controller.

system configuration by allowing you to set all of the floppy-disk-drive select jumpers to address 1, but it negates the original floppy-disk-drive cable's ability to address four drives. **Fig 3** illustrates how the Compaticard IV circumvents IBM's eccentric floppy-disk-drive cable limitations by splitting the four drives under its control into two pairs. Each pair of floppy-disk drives connects to the controller with a separate floppy-disk-drive cable.

However, solving the hardware limitations of IBM's floppy-disk-subsystem design doesn't fix the second problem—BIOS (basic I/O system) limitations. Most PC mother-board BIOS ROMs control only two floppy-disk drives. Although the Compaticard IV manages as many as four floppy-disk drives, IBM's original PC/AT computer did not. Consequently, computers and BIOS ROMs patterned after the PC/AT support only two floppy-disk drives. MicroSolutions skirted this problem by incorporating a floppy BIOS ROM on the Compaticard IV and supplying a loadable device driver for the extra two drives. The device driver adds the extra floppy-disk drives onto the end of the existing drive-designator chain. Thus, if your system has four floppy-disk drives and two hard drives, the first two floppy designators are A and B, the hard-drive designators are C and D, and the third and fourth floppy designators are E and F. This scheme works for most PCs, but can cause problems for systems that use enormous hard-disk drives and older versions of DOS.

This is not merely a hypothetical problem. The All-Star PC includes a pair of enormous hard-disk drives and initially used Microsoft's DOS 3.3, which accommodates disk drives with capacities to 32M bytes. The All-Star PC's hard-disk drives have a formatted capacity of 330M bytes each. DOS 3.3's solution to this mismatch was to create 10 logical drives out of each physical drive. As a result, the first hard-disk drive transmuted into logical drives C through L; the second hard-disk drive became drives M through V. The Compaticard IV therefore assigned designators W and X to the second pair of floppies. DOS only handles 26 logical drives (A through Z), leaving only two drive designators for use with other storage devices. Because the All-Star PC was going to have an optical WORM disk drive, there was actually only one drive designator left to play with.

Designator-related problems arose with a disk-caching program called PC-Cache, part of the PC Tools De-

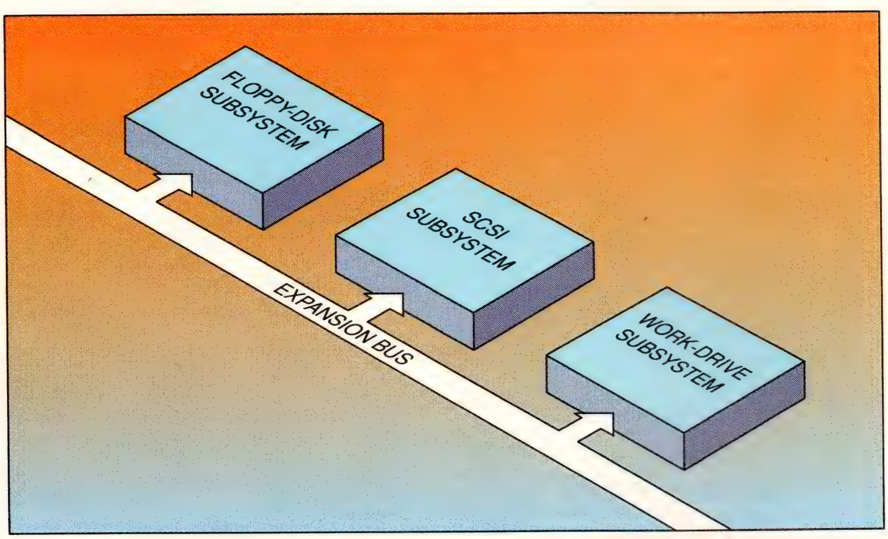


Fig 1—Three subsystems provide the All-Star PC's mass-storage capabilities: a floppy subsystem, a SCSI subsystem, and a WORM (write-once, read-many) optical-disk subsystem.

Sculpture by Kathy Jeffers/Sculpture Photography by Chris Vincent. Photography by The Photo Works and Steven Leibson unless otherwise noted.

luxe software package from Central Point Software Inc (Beaverton, OR, (503) 690-8090). PC-Cache improves hard-disk performance, but it interfered with the Compaticard IV's floppy-disk device driver. After loading the program, I could no longer read or write from the two 3½-in. floppy-disk drives, W and X. Suspecting that the cache program was interfering with the device driver, I instructed PC-Cache to ignore drives W and X. It couldn't, however, because it recognized only the first 16 drive designators, A through P. Clearly, PC-Cache and DOS 3.3 could not be used together on the All-Star PC. You'll find the solutions to this problem in Part 4.

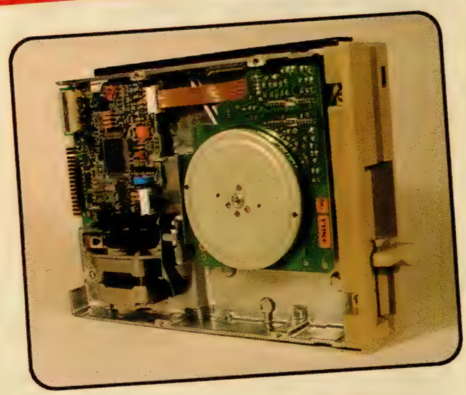
As long as PC-Cache wasn't activated, the floppy-disk drives worked fine. Even without a caching program, the All-Star PC's hard-disk drives, a pair of Seagate Technology's SCSI-based Wren Runners, are very fast. The hard-disk drives have an average-seek-time rating of 12.8 msec and a maximum track-to-track seek-time rating of 4.8 msec. (Both ratings include controller overhead.) They also support SCSI transfers at burst rates to 4.7M bytes/sec for synchronous transfers and 2M bytes/sec for asynchronous transfers. The All-Star PC could have used drives with larger capacities (some 5¼-in. SCSI hard-disk drives such as Micropolis Corp's 1590 series now have capacities in excess of 1G byte), but we couldn't find any 5¼-in. hard drives that were faster than the Wren Runners. For this project, speed reigned over capacity, because a pair of 330M-byte drives seemed to provide all the capacity the All-Star PC required.

No sane system integrator would omit a way to back up 660M bytes of on-line data. Because the Wren Runners employ SCSI I/O, I planned to use a SCSI-based tape drive that could back up both hard-disk drives on just one tape cartridge. These constraints left only one choice: Exabyte's EXB-8200 cartridge-tape subsystem. I briefly considered using a DAT (digital audio tape) drive, but one wasn't available in time for this project. The EXB-8200 stores 2.5G bytes on one 8-mm videotape cartridge, yet the entire unit, including an integral formatter/controller, occupies the space of a full-height, 5¼-in. drive. It also employs helical-scan recording.

The Wren Runners and the EXB-8200 require a SCSI host adapter for operation, but because of expediency (or perhaps because of a lack of foresight), the PC's BIOS only works with a Western Digital WD1003 controller card and ST-506 hard-disk drives. Tape drives are somewhat less trouble because PC BIOS ROMs don't support them at all. Therefore, there are no compatibility problems to overcome. PC disk controllers that don't imi-

EDN's PC All-Stars FD-55GFR 5¼-in. Mini Floppy-Disk Drive

Teac America Inc, 7733 Telegraph Rd, Montebello, CA 90640. (213) 727-7682.
Circle No. 667



STATS:
CAPACITY (unformatted): 1.6M, 1M bytes
CAPACITY (formatted, DOS): 1.2M, 360k bytes
TRANSFER RATE: 500k, 300k, 250k bps
TRACK DENSITY: 96 tpi
AVERAGE ACCESS TIME: 94 msec
SIDES: 2

BIO: The FD-55GFR reads and writes two DOS floppy formats: 1.2M and 360k bytes. It achieves these capacities while running at 300 rpm. In addition, the drive supports a second spindle speed, 360 rpm, for compatibility with the original PC/AT, but EDN's All-Star PC doesn't use this feature.

tate the PC/AT's original disk controller card do have compatibility problems. However, the rewards of using the SCSI bus are worth the risks of incompatibility.

Table 1—Compaticard IV floppy-disk formats

Drive Type	Formatted capacity (bytes)	Sides	First supported in DOS version:
5¼ in. 48 tpi 2 sided	360k	2	2.00
	320k	2	1.10
	180k	1	2.00
	160k	1	1.00
5¼ in. 96 tpi 2 sided	800k	2	Proprietary to Compaticard
	360k	2	2.00
	320k	2	1.10
	180k	1	2.00
	160k	1	1.00
5¼ in. 96 tpi 2 sided High capacity	1.2M	2	3.00
	800k	2	Proprietary to Compaticard
	360k	2	2.00
	320k	2	1.10
	180k	1	2.00
	160k	1	1.00
8 in. 2 sided	1.2M	2	Proprietary to Compaticard
	250k	1	1.00
3½ in. 2 sided	720k	2	3.20
3½ in. 2 sided High capacity	1.4M	2	3.30
	720k	2	3.20
3½ in. 2 sided Exended density	2.8M	2	Proprietary to Compaticard
	1.4M	2	3.30
	720k	2	3.20

SCSI provides many benefits

SCSI compatibility gives you a wide choice of high-performance storage peripherals, including hard-disk drives with a range of capacities (from less than 100M bytes to more than 1G byte), high-capacity floppy-disk drives, and tape drives. One industry group, the CAM (Common Access Method) Committee, is developing specifications to solve the driver problems for SCSI-based products, but the All-Star PC needed a SCSI host adapter that would work with the software and the storage peripherals immediately, not when CAM-compatible products finally appear (see **box,** "CAM: A common access method for SCSI").

There were two criteria for selecting the SCSI host adapter: speed and compatibility. Because the Wren Runners are so fast, a slow host adapter would introduce a bottleneck in the SCSI subsystem. And the compatibility objec-

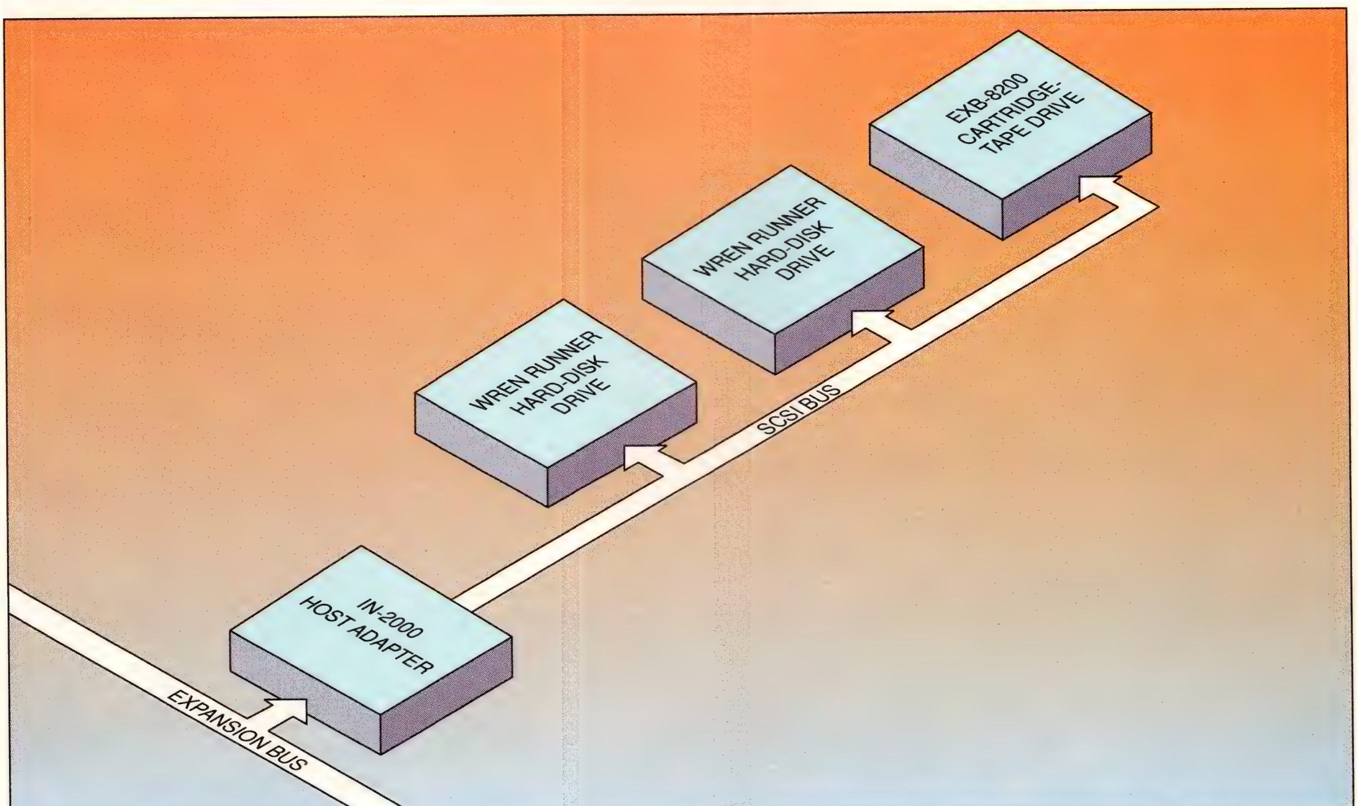


Fig 2—One SCSI host adapter, an IN-2000 from Always Technology, controls the All-Star PC's two 330M-byte hard-disk drives and the cartridge tape drive.

tive presented an even more complex problem. The SCSI firmware and software supplied with the host adapter had to be compatible with the variety of DOS extenders and operating systems that the All-Star PC would use. In addition, the host adapter had to support the Wren Runners and the Exabyte EXB-8200.

After testing host adapter cards from several manufacturers, I selected Adaptec's AHA-1540A. The AHA-1540A employs first-party DMA to achieve high transfer speeds. Even after confining the AHA-1540A to its slowest DMA transfer rate to prevent it from overrunning the All-Star PC's memory subsystem, it still achieved transfer rates of almost 1.3M bytes/sec, according to version 2.8 of a disk-performance test program from Core International (Boca Raton, FL, (407) 997-6055). However, after installing Quarterdeck Office Systems' (Santa Monica, CA, (213) 392-9701) QEMM memory manager, problems arose, which eventually forced me to choose an alternative SCSI host adapter (see **box,** "Lost in (memory) space").

Climbing out of the box

The lessons learned from working with the AHA-1540A led away from SCSI host adapters that employed first-party DMA. EDN Regional Editor Maury Wright helped find a product that offered format compatibility with the AHA-1540A (eliminating the need to reformat

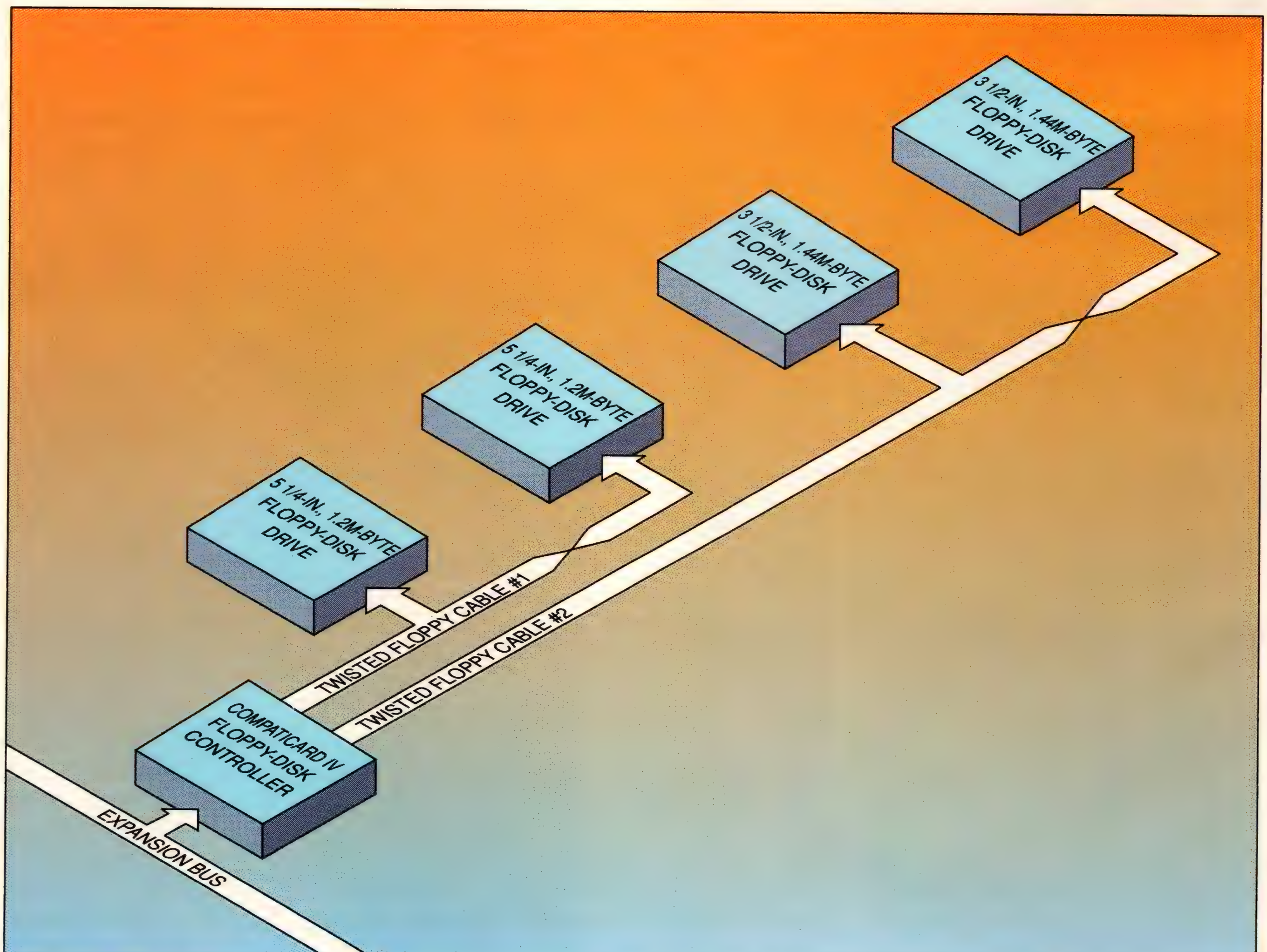


Fig 3—The PC's twisted floppy-disk cable can only handle two floppy-disk drives, so the All-Star PC's floppy-disk controller employs two such cables to control its four floppy drives.

the hard-disk drives), had the requisite operating-system and device drivers available, didn't use first-party DMA, and promised good performance. That product is Always Technology's IN-2000 AT SCSI Host Adapter.

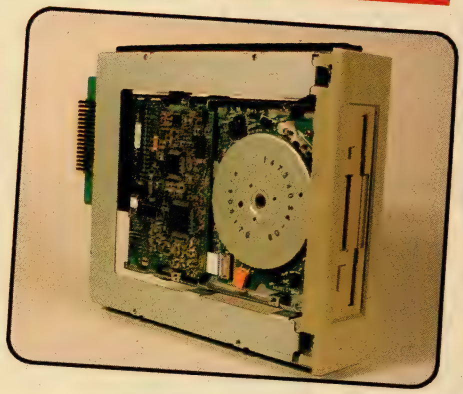
Once installed in the All-Star PC, the IN-2000 worked as advertised. The machine booted without reformatting the hard-disk drives. In addition, the board proved compatible with QEMM's memory-mapping abilities, indicating that the first-party DMA problem was indeed solved. However, after a keyboard reset (invoked by pressing the control, alt, and delete keys simultaneously), the PC locked up shortly after initializing the SCSI drives. Always quickly determined that the problem was caused by the consecutive SCSI addresses I used for the hard-disk and tape drives. Moving the tape drive to SCSI address 4 solved the problem by separating the tape drive and the hard-disk drives at addresses 0 and 1. Without the address gap, the IN-2000 was attempting to initialize the tape drive as if it were a disk drive, and as a result, locked up.

The Core test claimed that the IN-2000 initially transferred 970k bytes/sec, roughly 25% less than the AHA-1540A. This is a respectable speed, but the Wren Runners can do better, as earlier experiments with the AHA-1540A proved. A search for the I/O bottle-

EDN's PC All-Stars FD-235HF 3½-in. Micro Floppy-Disk Drive

Teac America Inc, 7733 Telegraph Rd, Montebello, CA 90640. (213) 727-7682.

Circle No. 668



STATS:
CAPACITY (unformatted): 2M, 1M bytes
CAPACITY (formatted, DOS): 1.44M, 720k bytes
TRANSFER RATE: 500k, 250k bps
TRACK DENSITY: 135 tpi
AVERAGE ACCESS TIME: 94 msec
SIDES: 2

BIO: The FD-235HR weighs little more than ½ lb and measures exactly 1 in. high, yet it can store more than 1M byte of data on a floppy disk.

CAM: A common access method for SCSI

The PC's lack of adequate drivers for SCSI host adapters and peripherals caused many of the All-Star PC Project's mass-storage problems. Peripheral vendors rely on host-adapter vendors to write the peripheral drivers because those drivers are always specific to the host adapter. The host-adapter vendors can't possibly write software drivers for every conceivable SCSI peripheral; they're too busy writing drivers that couple their boards to the most popular PC operating systems. Consequently, every SCSI host adapter for the PC works with only a few PC operating systems and supports only a subset of the available peripherals. The CAM (Common Access Method) Committee is trying to eradicate this problem.

Formed in 1988, the committee is developing several specifications that will allow vendors to write one set of drivers for every operating system, host adapter, and peripheral device. It includes representatives from a wide cross section of peripheral, host-adapter, and computer vendors. Currently, the committee is focusing on the needs of PC systems, but the software-access methods it develops should be extensible to other computer systems as well.

For the PC, the committee is approaching the problem at the lowest level. Most PC operating-system software can control disk drives attached to a Western Digital WD1003 hard-disk controller because that is the controller IBM shipped with the PC/AT. The CAM Committee's ATA (AT Attachment) spec defines a standard method that allows SCSI host adapters to mimic the WD1003 by emulating its register set. This approach eliminates the need for special SCSI drivers. Perceptive Solutions Inc (DeSoto, TX, (214) 224-6774) offers a caching disk controller, the Hyperstore 1600, that has a WD1003 emulation mode along the lines of CAM's ATA spec. The committee is also developing an enhanced AT attachment (EATA) specification that allows a driver to take advantage of SCSI features not available through the ATA emulation mode. For more information about the CAM Committee, contact its chairman, I Dal Allen, 14426 Black Walnut Ct, Saratoga, CA 95070. Phone (408) 867-6630.

neck (with the intent of boosting the SCSI subsystem's performance), coupled with two experiments, exposed the culprit. For the first experiment, Always supplied a revised BIOS ROM for the IN-2000 that reprogrammed the board's SCSI protocol chip, a Western Digital WD33C93, to eliminate handshake delays that the chip was generating. Always put the delays in as a conservative measure, though they weren't needed. Eliminating those delays boosted the IN-2000's Core test results to almost 1.3M bytes/sec, tying the AHA-1540A.

Exonerating the expansion bus

The second experiment took place at Cheetah International, where, after plugging the original BIOS ROM back into the IN-2000, we changed a PLD on the Cheetah Gold 425 mother board to speed its expansion bus from 6 to 8 MHz. That experiment had no effect on the Core test, proving that the "slow" ISA bus was not interfering with the All-Star PC's disk-transfer-rate efficiency. Of course, absolute test numbers don't tell you very much about a computer system, but these two experiments demonstrate a valid use for benchmarks. The All-Star PC won't in all likelihood consistently transfer data over the SCSI bus at 1.3M bytes/sec for every application, no matter what Core's test results say. However, in carefully controlled experiments such as the two described above, the Core benchmark provided relative performance data that helped improve the All-Star PC's performance.

With the SCSI performance problem supposedly licked, I loaded a suite of tape-backup-software programs, supplied by Novastor Corp (Westlake Village, CA, (818) 707-9900), onto the system. When the All-Star PC tried to run the Novastor programs, every one locked up the computer. Frantic calls to Novastor and Always Technology resulted in the discovery that the Novastor files on the hard disk were corrupted; they simply didn't match their counterparts on the floppy disks. Further testing revealed that the IN-2000 SCSI host adapter with the new BIOS ROM was no longer writing data to the disk correctly.

Lost in (memory) space

DMA controllers have a tough time working with µPs that incorporate on-chip memory-management units, especially if the code running the DMA controller doesn't know that address translation is occurring. This scenario occurs when you use DOS extender programs, such as Quarterdeck's QEMM memory manager, in conjunction with expansion cards that employ first-party DMA. QEMM can map blocks of extended memory (located above 1M byte in the µP's address space) into unused address spaces below 1M byte, and it can also switch extended memory into the program area—between 0 and 640k bytes—for multitasking operations.

QEMM handles mother-board DMA transfers by providing a protected buffer area, but this technique won't work for first-party DMA controllers that are not aware of QEMM. DOS is ignorant of memory management and provides no way for QEMM to tell it that logical memory addresses no longer match physical addresses. Most DOS services don't need to know about remapped addresses. However, DOS manages first-party DMA controllers and supplies them with the destination addresses for transfers. If logical and physical addresses no longer correspond, the first-party DMA controller will write data into the wrong physical addresses, which is exactly what happened to the All-Star PC when it used Adaptec's AHA-1540A.

Quarterdeck and Phar Lap Software Inc (Cambridge, MA, (617) 661-1510) jointly developed, published, and support a specification that allows software such as a disk BIOS to find out how memory has been mapped by the DOS-extension program. This specification, called the VCPI (Virtual Control Program Interface), provides a function call that supplies the logical-to-physical address-mapping information.

VCPI has become a de facto standard that several major software vendors support. Adaptec's software doesn't support VCPI. Instead, it creates a buffer for DMA transfers when they are used with DOS extenders. Invoking this feature of Adaptec's driver carves 64k bytes from DOS's already overcrowded 640k program space. Although you can shrink the size of Adaptec's DMA buffer (resulting in a speed reduction), I judged this solution to be inadequate for the All-Star PC's needs and reluctantly benched the AHA-1540A.

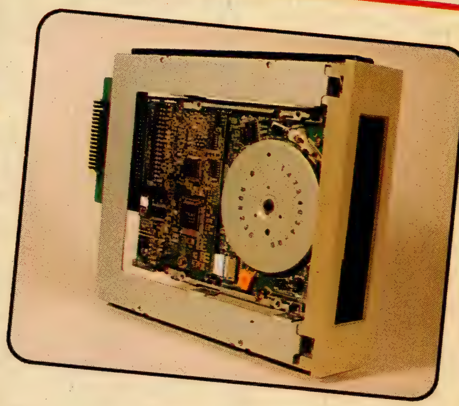
Johan Olstenius, the IN-2000's designer, discovered a logic path on the host adapter that was too slow to handle the faster SCSI transfers. Fortunately, the IN-2000 employs Xilinx field-programmable gate arrays (FPGAs) for most of the board's logic, so the correction required only a ROM change. A small EPROM on the IN-2000 holds the FPGA configuration information, which is loaded automatically by the Xilinx parts at power up. Olstenius rewired some of the circuitry in the Xilinx chip to speed up the slow logic path. This exercise underscores the advantages of the "soft hardware" design approach employed on the IN-2000. I plugged in the new configuration ROM, and after reinstalling the tape software, backed up the information on the hard disks.

EDN's All-Star PC incorporates a second type of storage peripheral that provides archival storage: an APX-5000 optical-disk subsystem from Maximum Storage Inc. The APX-5000's WORM optical-disk cartridge stores more than 500M bytes on each side for a total capacity of approximately 1003M bytes. You may wonder why the All-Star PC has a WORM drive when it already has the Exabyte tape drive. Both the Exabyte and Maximum

EDN's PC All-Stars **FD-235J 3½-in. Micro Floppy-Disk Drive**

Teac America Inc, 7733 Telegraph Rd, Montebello, CA 90640. (213) 727-7682.

Circle No. 669



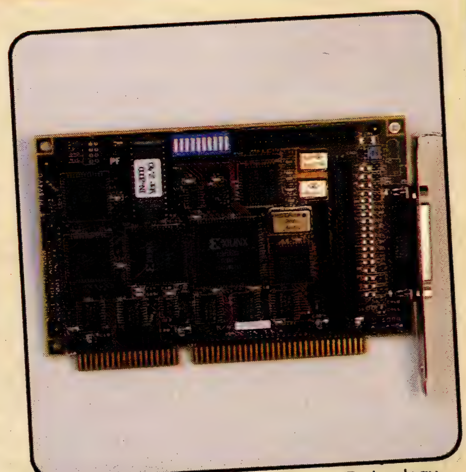
STATS:
CAPACITY (unformatted): 4M, 2M, 1M bytes
CAPACITY (formatted, DOS): 2.8M, 1.44M, 720k bytes
TRANSFER RATE: 1M, 500k, 250k bps
TRACK DENSITY: 135 tpi
AVERAGE ACCESS TIME: 94 msec
SIDES: 2

BIO: The FD-235J stores 2.8M bytes of formatted data on special barium-ferrite media while maintaining read and write compatibility with earlier 3½-in. floppy-disk drives.

EDN's PC All-Stars **IN-2000 AT SCSI Host Adapter**

Always Technology, 31336 Via Colinas, Suite 101, Westlake Village, CA 91362. (818) 597-1400. FAX (818) 597-1496

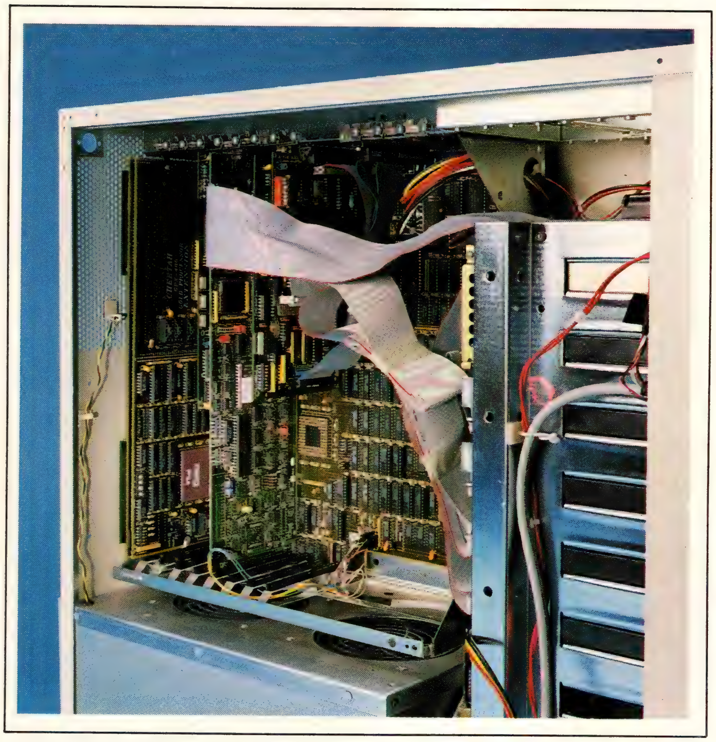
Circle No. 670



Always Technology

STATS:
BUS: ISA (PC/AT)
BUS-TRANSFER MODE: 16-bit programmed I/O
COMPATIBILITY: INT 13H BIOS calls
BIOS ADDRESS: Selectable
CONNECTORS: Internal and external SCSI
EXTRA FEATURE: AT-style floppy-disk controller

BIO: Each IN-2000 host adapter controls as many as seven SCSI peripherals. You can plug four IN-2000s in a system for a maximum system capacity of 28 SCSI devices.



Even with just the SCSI and floppy cabling in place, the interior of the All-Star PC is becoming a rat's nest of wiring.

Storage drives can back up the All-Star PC's two 330M-byte hard-disk drives with one cartridge. Four key factors differentiate the tape and WORM drives: the tape drive stores more data per tape cartridge than the WORM drive stores on a disk cartridge; the tape cartridges cost much less than the optical-disk cartridges; the WORM drive provides much faster access to data than the tape cartridge; and the WORM drive provides indelible storage.

Storage on the tape drive costs less per byte, making tape a better alternative for backup storage, which retains information as an insurance policy against a hard-disk crash. Although the Maximum Storage WORM drive could satisfy the need for backup storage, you would quickly fill up the relatively expensive and nonerasable WORM cartridge if you used it for daily or even weekly backups. However, the indelible storage and higher speed of the WORM drive provide many benefits to a PC-based (or any other) workstation that are not related to backup storage but to archival storage. Archival storage holds files that you wish to save but don't necessarily need to have immediately at hand.

For example, you could use the WORM disk cartridge to freeze a suite of design and development software in case you ever need to revert to that particular version. Sad stories abound of engineers who needed to revise a design, only to discover that the particular versions of the CAD and CAE software tools required for editing the old design files were long gone. A 1G-byte WORM cartridge allows you to save several down-level versions of your favorite software tools. You can be confident that those files cannot be erased to make room for newer software. The same advantage applies to different versions of your design

What's missing?

The All-Star PC incorporates eight storage peripherals, but some device types are conspicuously absent. An erasable optical disk drive wasn't included for two reasons. First, optical disks are not standard methods for data interchange among PCs; second, the Exabyte and Maximum Storage drives provide all the archival and backup storage the All-Star PC needs. Also omitted is a CD ROM drive, because the use of such drives is still very application specific. For example, Cahners's Technical Information Service (Newton, MA, (617) 558-4960) provides a comprehensive electronic device catalog called CAPS (Computer-Aided Product Selection) on CD ROMs and supplies you with the CD ROM drives when you subscribe to the CAPS service.

Also missing from the All-Star PC's mass-storage menagerie is a network connection—not because networks lack merit, rather, because of realistic constraints on the project. With only one machine, there is simply no way to test a network card.

specifications and your designs. Maximum Storage provides tools for version control as you update files. You can always retrieve an older version of a file from the WORM disk cartridge.

The APX-5000 is an external unit. The All-Star PC uses an external unit for two reasons. First, it has no more drive bays to accommodate a WORM disk drive. Second, in an environment where engineers may have an irregular need for the capabilities of the WORM disk drive, the external drive can be passed around. You can plug a Maximum Storage controller board into each engineer's workstation and share the drive. That configuration costs much less than equipping every engineering workstation with a WORM drive.

Maximum Storage developed its own file-storage system instead of using the DOS file structure, so its APX-5000 works on a variety of computer systems and workstations. The common file format across multiple computers makes the ability to move the drive from system to system even more attractive because the APX-5000's disk cartridge becomes a good medium for data interchange among otherwise incompatible systems.

The APX-5000 drive has an ESDI (Enhanced Small Device Interface) port, so it doesn't work on the SCSI bus. Maximum Storage supplies a proprietary disk-controller card for the drive. The APX-5000, when

EDN's PC All-Stars Wren Runner 5¼-in. Rigid-Disk Drive

Seagate Technology, 920 Disc Dr, Scotts Valley, CA 95066. (408) 438-6550. FAX (408) 438-4127. **Circle No. 671**

STATS:
CAPACITY (unformatted): 385M bytes
CAPACITY (formatted, 512-byte sectors): 338M bytes
AVERAGE DATA-TRANSFER RATE: 15.5M bps
AVERAGE SEEK TIME: 10.7 msec
INTERFACE: SCSI
STORAGE METHOD: Zone bit recording

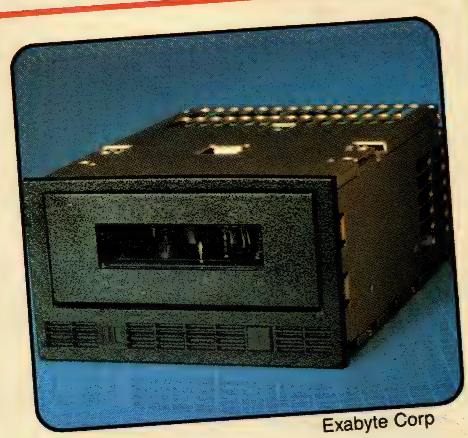

Seagate Technology

BIO: The Wren Runner achieves its fast average-seek time by limiting the area on the disk used for storage. Zone bit recording gives the drive high capacity even with the reduced storage area.

EDN's PC All-Stars EXB-8200 8-mm Cartridge Tape Subsystem

Exabyte Corp, 1745 38th St, Boulder, CO 80301. (303) 442-4333. FAX (303) 442-4269. TLX 361740. **Circle No. 672**

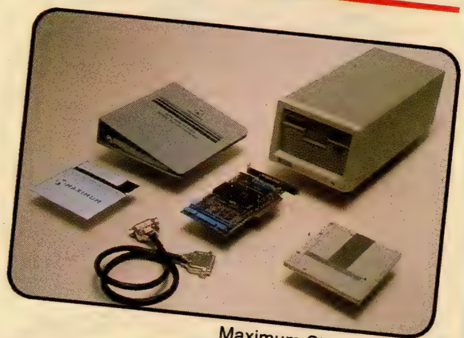
STATS:
CAPACITY: 2500M bytes
DATA TRANSFER RATE (peak): 1.5M bytes/sec
DATA TRANSFER RATE (average): 246k bytes/sec
TAPE SPEED: 0.429 ips
CARTRIDGE: Standard 8-mm videotape
INTERFACE: SCSI


Exabyte Corp

BIO: The EXB-8200 can store more than 2500M bytes on a standard 8-mm videocassette tape. It fits in a 5¼-in., full-height peripheral bay.

EDN's PC All-Stars **APX-5000 Optical-Disk Subsystem**

Maximum Storage Inc, 5025 Centennial Blvd, Colorado Springs, CO 80919. (719) 531-6888. FAX (719) 531-0227.
Circle No. 673



Maximum Storage Inc

STATS:
CAPACITY: 1003M bytes
DATA TRANSFER RATE: 5M bps
EFFECTIVE AVERAGE ACCESS TIME: 28 msec
CARTRIDGE: 2-sided, removable
INTERFACE: Modified ESDI
DISK CONTROLLER: Proprietary

BIO: The APX-5000 stores more than 500M bytes on each side of its WORM (write-once, read-many) optical-disk cartridge. It is available in both internal-mount and external versions for PCs.

first plugged into the All-Star PC, didn't work. The controller had trouble communicating with the drive. However, turning off the 80486 µP's internal cache RAM cured the problem. That clue pointed an accusing finger at the APX-5000's device-driver software. In many high-speed PCs, the expansion-bus's speed may cause problems. However, the All-Star PC's expansion bus runs at 6 MHz specifically to avoid such problems.

Barry Bremsteller at Maximum Storage discovered the problem's cause. The driver routines that monitored the proper operation of the controller card were timing out before the hardware had time to execute its commands. The culprit proved to be the delay function in Borland International's (Scotts Valley, CA, (408) 439-1800) Turbo C function library. The delay routine is self- calibrating over a range of µP speeds, but the 80486 simply burst past the limits of the self-calibration algorithm. The company has fixed the delay function in its Turbo C and Turbo Pascal libraries and you can get that revised library code from Borland.

With the device driver fixed, the APX-5000 worked flawlessly and the All-Star PC's complement of mass-storage devices was complete. That still left the machine deaf, mute, and blind. EDN

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4. Leibson, Steven H, "Optical-disk drives target standard 5¼-in. sites," *EDN*, December 25, 1986, pg 42.
5. Terry, Chris, "Rewritable optical-disk drives, optical units provide mass storage," *EDN*, May 11, 1989, pg 59.

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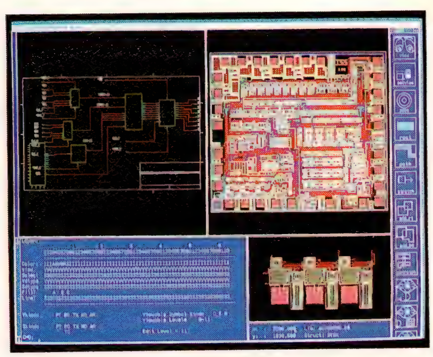

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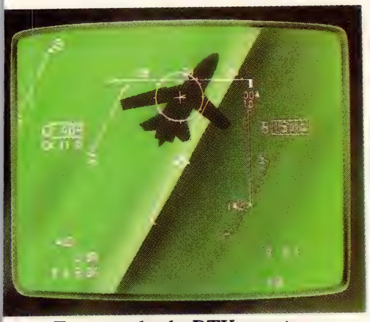
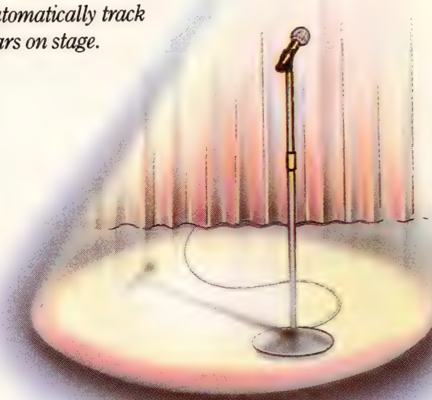
ime real fast.



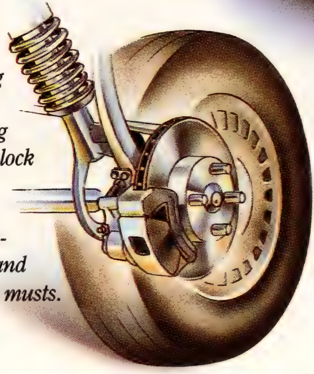
For example, the RTX executes typical image processing applications up to an order of magnitude faster than CISC or RISC chips.

The RTX doesn't just track aircraft in target ID systems. It's also being used to automatically track stars on stage.

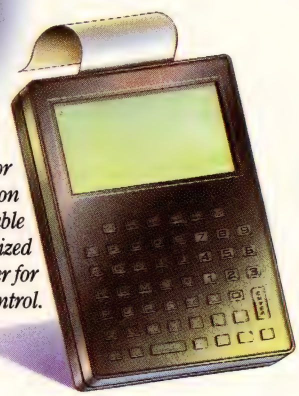


The RTX has near-zero power consumption in standby, thanks to static CMOS technology. That's how the life of these remote data acquisition buoys was extended from one month to one year.

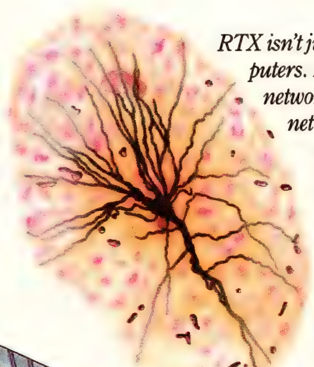
The RTX is a driving force in automotive applications, including engine controls, anti-lock braking, and active suspensions, where high-integration, low-power consumption and high performance are musts.

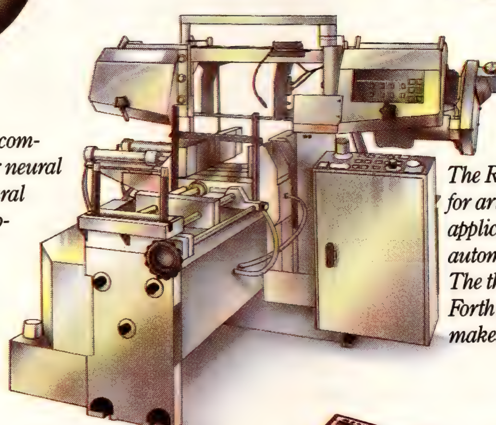


The RTX's form factor and low-power consumption make it ideal for portable applications like this ruggedized handheld computer for inventory control.

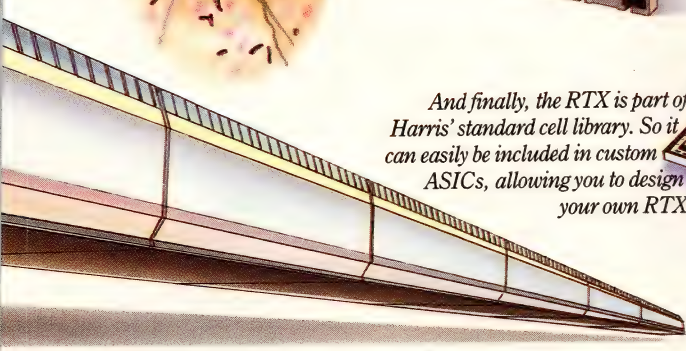


RTX isn't just for ordinary computers. It's also ideal for neural networks. A RTX neural net is under development for voice identification.

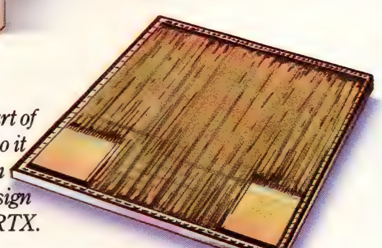




The RTX is also perfect for artificial intelligence applications like this automated lumber mill. The threaded nature of our Forth development system makes it ideal for AI.



And finally, the RTX is part of Harris' standard cell library. So it can easily be included in custom ASICs, allowing you to design your own RTX.



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CIRCLE NO. 69

Single-chip μPs tax ingenuity of C-compiler designers

Single-chip-μP designers never had high-level languages in mind, but high-level-language designers never had single-chip μPs in mind, either. The first part of this 2-part series contrasts how conventional C programs should work and how well single-chip μPs actually suit C. The second part will cover C extensions and optimizations tailored for specific single-chip μPs along with detailed programming tips for writing tight C programs.

No matter how many lines per second *your optimizing C compiler can crunch, it cannot make up for a bad algorithm.*

Charles H Small, *Senior Editor*

Despite all the hoopla about the latest, greatest RISC (reduced-instruction-set computer) and CISC (complex-instruction-set computer) μPs, engineers are writing more code for workhorse 8-bit single-chip μPs than any other kind of μP. Desperately seeking productivity improvements, these engineers are looking hard at optimizing C compilers as replacements for their assemblers.

Compiler enthusiasts cite a pseudoscientific IBM study, done years ago, that "proved" that programmers produce five times as much code per day when writing in high-level languages compared with writing in assembly languages. Even if the study had proven that claim true, software engineers could well wonder if such quickly produced code is as good as their handcrafted assembly-level programs.

Well, to be fair, optimizing C compilers for single-chip μPs produce object code that's almost as tight as an equivalent hand-coded program would be if—and this is a mighty big if—the hand-coding programmer were somehow forced to write a program that executes as a C program does (**Fig 1**). Obviously, this assertion begs the question of whether software engineers really want to routinely run C-style programs in their single-chip μPs (see **box,** "What is C's style?").

Unfortunately, a couple of flies are buzzing in this soothing Brand C ointment. The most loudly buzzing

Software engineers wonder if quickly produced code is as good as hand-crafted assembly-level programs.

fly is the poor match between the assumptions C makes about computers and the real nature of common 8-bit single-chip μPs.

For example, the C mechanisms for modularity and re-entrancy assume that the target processor actually has a stack of respectable size and some mechanisms for manipulating the stack. After all, the functions of a modular, re-entrant C program—by design—thrash the stack continuously. CISC μPs, such as the 68000 family, actually have special instructions for setting up and tearing down stack frames in addition to stack-pointer-relative addressing.

Garden-variety single-chip μPs, on the other hand, not only don't have specialized stack instructions that accommodate high-level languages, most of them have barely enough stack space to hold a few subroutine call-return parameters for the hardware. For example, the indexed-load instruction of the Z80 core of the 64180 and Z180 single-chip μPs has a range of only ±127 bytes. (Z-World's C compiler uses this instruction for stack-frame pops.) Because the 8051's hardware has a minuscule internal stack, C-compiler designers often maintain a simulated software stack in its main memory for some, or all, C operations. This off-board software stack is slow compared with the hardware stack.

When you run your C program on a big computer, you can speed up execution by directing the compiler to put some often-used variables in registers instead of in main memory or on the stack. Some compilers for single-chip μPs will cheerfully accept such directives and then . . . do absolutely nothing! The problem is

What is C's style?

C's designers wanted a language that produced modular, re-entrant object code. In fact, C's modularity, rather than its high-level syntax, accounts for most of its software-productivity gains over assembler. Software engineers can quickly and easily—some might say *too* easily—plug a multitude of prewritten functions into their programs.

As **Fig A** shows, to be modular and re-entrant, each C function should, upon entry, make room on the stack for its local variables in a "stack frame." If the function calls another function, the first function should also push copies of the parameters it's passing to the called function on the stack before exiting. The called function, in turn, sets up its own local variables on the stack and copies the passed parameters from the stack as it needs them. Upon exit, the called function deallocates its local-variable storage and returns any results to the calling function on the stack.

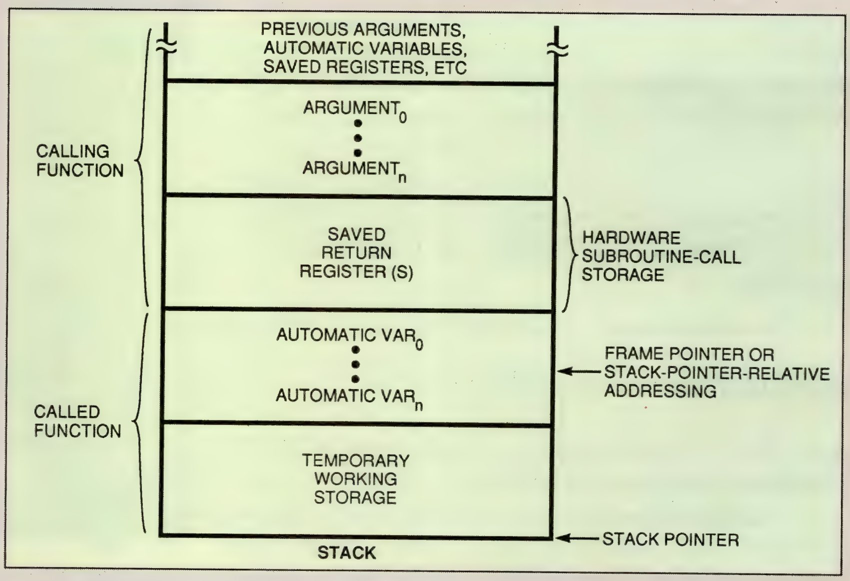

***Fig A—Each function in a classical C program** uses the stack for temporarily storing local variables, or "automatic variables," and passing parameters to called functions.*

This way, all functions use the same mechanism for passing information back and forth (modularity) and each entry into a routine creates a new set of passed information and local variables (re-entrancy). A function can even call itself with impunity. Thus, different threads of execution can use the same function over and over, or simultaneously, without interfering with each other. If the function kept a single copy of these items in memory, the function would not be reentrant or as modular.

```
0010 0011 0012 0013 0014 0015      unsigned int a,n,m,o,p,q;
0016 000A                          int e[10];
0020 000A                          int f[10];
002A                               int i;
                                   main ()
                                    {
0100 3F 11      CLR     $11           for (n=0;n<m;n++)
0102 B6 11      LDA     $11
0104 B1 12      CMP     $12
0106 24 13      BCC     $011B
                                       {
                                        if (e[o=(f[5+n] & 0xf0)>>1])
0108 97         TAX
0109 E6 25      LDA     $25,X
010B A4 F0      AND     #$F0
010D 44         LSRA
010E B7 13      STA     $13
0110 97         TAX
0111 E6 16      LDA     $16,X
0113 27 02      BEQ     $0117
                                        {
0115 3C 15      INC     $15              q++;
                                        }
                                       }
0117 3C 11      INC     $11
0119 20 E7      BRA     $0102
011B 81         RTS                 }
```

Fig 1—This C code fragment for a 6805 *came from a real program. The **if** statement makes a decision based on a variable stored in array **e**. The expression containing **f** indexes array **e**, offset by both a constant and a variable amount. Variable **o** stores the result of this calculation. Notice both the order in which the compiler performs these operations and the instructions it selected. You can judge for yourself how much more productive you'd be writing code like this in C instead of assembler. (Listing courtesy Byte-Craft)*

that the compiler has already used up all of the tiny processor's internal registers for its own housekeeping and doesn't have any room left over for your variables.

Lumpy properties

Single-chip μPs are "lumpy" rather than smooth and homogeneous. They have numerous properties that change dramatically, by fixed quanta, when you exceed some limit or cross some boundary. Their instruction sets are quirky and irregular. For example, the Z80 core of the 64180 and Z180 single-chip μPs has good instructions for comparing 16-bit unsigned numbers, but poor instructions for comparing signed numbers. Non-ANSI C assumes that all integers are signed integers.

Some single-chip μPs perform 8-bit math, 8-bit logic operations, and 8-bit memory addressing much faster than equivalent 16-bit operations. For example, single-chip μPs of the Motorola 68xx family operate much faster out of the lowest page, or "zero page," of their memories. Some of the 6805's instructions—the bit-manipulation instructions, for example—don't even have a counterpart in the address space above location 255. C, on the other hand, has no operators for 8-bit math or memory addressing; it frequently "promotes" 8-bit values to 16 bits automatically during computations and logic operations.

Single-chip μPs often have multiple memory spaces and a mind-numbing panoply of built-in hardware. C has only one way to address memory because the language assumes that the target computer has a uniform address space and instruction set. C is ignorant of the concept of memory-mapped hardware.

C wants to be portable. Therefore, it has only a few operators and dedicated keywords. Single-chip μPs have specialized instructions for dealing with their built-in hardware and for performing operations peculiar to embedded processing. In other words, you can utter statements in C that single-chip μPs cannot easily execute, and the μPs have useful instructions that have no corresponding standard C expression.

Stranger in a strange land

Unlike Forth, another popular high-level language for single-chip μPs, C is not extensible. Thus, software engineers cannot add specialized operators to C, as they can with Forth, to handle the special needs of single-chip μPs and embedded systems. For example, in embedded-systems programming, software engineers often know the range of the input variables they

Optimizing C compilers for single-chip μPs produce code that's almost as tight as an assembly program would be if it were done in C style.

can expect. Thus, they can use much faster and more compact integer math rather than slow, cumbersome floating-point math.

Forth has a series of compound math operators, the utility of which would mystify the average high-level language programmer. But these operators prove invaluable for integer math because they scale and manipulate integer data. To preserve accuracy, these operators save a double-precision intermediate result. For example, the compound operator "*/" multiplies an integer number by an integer fraction. It first multiplies the datum by the numerator, which generates a double-precision intermediate result. It then divides this double-precision result by the denominator returning a single-precision final result.

The best way to perform such operations in C would be to momentarily drop out of C and insert an assembly-language macro into your program every time you needed to scale an integer datum **(Fig 2)**.

However, the portability of your C code takes a double hit if you insert assembly-language macros. First, each single-chip μP obviously has its own instruction set. Thus, you'll have to rewrite the assembly-language macros if you want to recompile your program for another single-chip μP. Less obviously, each C compiler from competing compiler vendors has its own subtly different assembler syntax. So even if you want to compile your program for the same single-

```
long sum;
int step;

/* function to add  step to sum*/
stepsum()       {
#asm
        ld      hl,(step)
        ld      de,(sum)
        add     hl,de
        ld      (sum),hl
        jp      nc,@ret         ;if no carry to most sig
        ld      hl,(sum+2)
        inc     hl
        ld      (sum+2),hl
#endasm
return;
}
```

Fig 2—One way to work around C's lack of operators *for a single-chip μP's special instructions is to temporarily drop out of C and into assembly language. Here, the* ***#asm*** *preprocessor directive plunks some 64180/Z180 assembly code into the guts of the function* ***stepsum****. (Listing courtesy Z-World)*

chip μP, you may have to make many little changes in your macros if you change compilers.

C relegates to library programs what many languages have built in. This strategy can be a blessing or a curse. For example, C has no built-in I/O functions. Thus, you can write your own I/O routines—or you could call standard I/O functions from a program library and suddenly find that your program has grown by 10k bytes. Picking up 10k bytes here and 8k bytes there isn't much of a problem in the big-system world that C comes from. But overweight library routines exact real penalties in a single-chip-μP system's limited memory space.

For example, some C compiler vendors have a universal floating-point math package written in C. To target the package for a specific processor, they simply compile it with their own single-chip μP compiler. Other vendors write a floating-point math package in assembly language for each processor. Also, watch out for—incredibly enough—library routines that are not re-entrant.

C compilers for big systems often initialize all variables to zero at startup time. This custom can be a fatal mistake in an embedded system because it destroys the system's operating history whenever the system reboots. Further, C copies the "string pool" of defined messages to RAM upon start-up. In an embedded system, messages should stay in ROM. On a big system, C depends on an elaborate operating system for initialization and error handling. Embedded systems have no operating system to handle start-up, initialization, and errors. They must handle all these chores by themselves.

C doesn't concern itself with hardware. So the good news is that you *can* write your own routines to exploit the on-chip resources of single-chip μPs, such as counter/timers, communications ports, and A/D converters. The bad news is that you *have* to write these routines yourself unless the compiler vendor supplies usable library routines.

Further, unless your C compiler recognizes the new ANSI C preprocessor directive *volatile*, C is oblivious to the machinations of interrupt handlers. The single-chip μP's hardware can invoke interrupt handlers, which then steal, wraith-like, through the memory and change data values without telling the high-level program that its supposedly untouched variable values are actually built on shifting sands. And C has no mechanism to connect an interrupt to a particular interrupt-handling function.

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The C mechanisms for modularity and reentrancy assume that the target processor has a stack of respectable size and some mechanisms for manipulating the stack.

Compiler designers are hammering away at C to make it fit single-chip µPs and embedded-system programming. They've hidden some of their efforts in the bowels of their compilers as optimizations and alterations of C's basic schemata. Other efforts are visible to programmers as extensions of C's operators and data types. (Part two of this series will detail the second class of efforts.)

Optimization is a matter of bytes and microseconds. You can optimize for minimal bytes or minimal microseconds, but not often for both. Compiler optimizations come in two flavors: optimization of the C code (or an intermediate, nonprocessor-specific code) and optimizations done to tailor the code to a specific processor. (Part two will also detail this second flavor of optimizations.) All compiler designers have a suite of elementary optimizations that they apply to your C program willy-nilly during their compiler's first pass through your program if you turn on the compiler's optimizer option.

For example, the optimizers "fold" constants. The optimizer transforms *b = 3 + c − 5* into *b = c − 2*. The optimizer also simplifies algebraic expressions such as *a + 0* and *a / 1*. Although these examples look trivial, in practice such expressions typically result from preprocessor-defined terms and named constants. Another common optimization is jump-chain compression. The optimizer redirects jumps to other jump instructions into direct jumps to the final target.

C optimizers also convert logical expression into faster arithmetic operations. For example, if a software engineer writes *if (p = = 0)* ("= =" is the C equality operator), then the optimizer converts the statement into *if (!p)* ("*!*" is the C negation operator). Furthermore, the optimizer can transform tests such as *if (a && b || c != d)* ("&&" and "||" are the C logical-AND and -OR operators, respectively) into control flow statements, instead of evaluating each subexpression to a numerical result first.

Optimizers run riot

But be aware that these common optimizations come from the batch-processing, big-system world and some can actually foul up programs written for real-time systems. For example, optimizing compilers often remove "dead code." If the optimizer sees repeated writes to the same memory location without an intervening read, it assumes that all but the last write is redundant. Such an optimization can ruin a program if it's writing to a memory-mapped hardware register or device.

Optimizing compilers look for functions that never get called and loops and tests that do no useful work and eradicate them. Too bad for you if you have carefully crafted delay loops inserted at strategic points in your program—the optimizer happily eliminates your do-nothing timing loops.

Really smart optimizing compilers look for repeated computations of the same value in different parts of your program. Compiler designers call such operations common subexpressions. If the optimizer finds any common subexpressions, it assumes that the result will always be the same. It cuts all but the first calculation and uses the result from the first calculation repeatedly **(Fig 3)**. Here again, C betrays its lack of familiarity with interrupt handlers. Your program might be fetch-

(a)
```
func()
{
    int quit;
    extern int hw_reg;
        .
        .
        .
    do {
        .
        .
        .
    quit = hw_reg & 0x80;
        .
        .
        .
    } while (!quit);
}
```

(b)
```
func()
{
    int quit;
    extern int hw_reg;
        .
        .
        .
    quit = hw_reg & 0x80;
    do {
        .
        .
        .
    } while (!quit);
}
```

Fig 3—An optimizer, seeing a repeated calculation *involving the memory-mapped register* ***hw_reg*** *in* ***a****, mistakenly believes it can pull the calculation out of the loop* ***(b)****. The optimizer thinks that the contents of* ***hw_reg*** *will remain unchanged unless the processor writes to it. (Listing courtesy Z-World)*

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CIRCLE NO. 71

ing the latest value from a memory-mapped I/O device and not just reading the same memory variable over and over.

Optimizing compilers perform a similar optimization within loops, which is called loop-invariant optimization. If you poll a memory-mapped device in a loop, the optimizer might simplemindedly assume that you're reading the same value over and over from a memory location and move the memory access outside the loop. The optimizer thinks it's being really smart because with the memory access outside the loop, it gets executed only once.

Some optimizers unroll loops. Instead of jumping back to the beginning of the loop a given number of times, the compiler concatenates that many versions of the loop's body code. The tradeoff here is program length versus overhead consumed in indexing the loop.

Experienced C programmers have workarounds for all these possible problems. And—luckily—some veteran, real-time programmers sit on the ANSI C committee. Their input to the committee has resulted in the new C preprocessor directive, *volatile*. This directive tells the compiler not to assume that a variable will always have the same contents.

Additionally, ANSI C is more strongly typed than old C. For example, if you declare p to be a pointer to type T, p won't modify anything but targets of type T. If a pointer can point to any type of object, then a compiler designer can't perform much optimization on pointers.

Not all routine optimizations are potential sources of trouble. Some are just good programming practice in automated form. For example, all compilers rearrange *for* loops by putting the test at the bottom of the loop instead of at the top of the loop. The lack of fit between ivory-tower, theoretical programming structures and the reality of how computers really work accounts for the popularity of this optimization.

And you can forget about the old assembly-language programmer's trick of substituting shifts and adds for multiplication or division by powers of 2; all optimizers already know that one. To find out what other assembly-language programmers' tricks C-compiler designers have incorporated, read part two of this series. EDN

Article Interest Quotient (Circle One)
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Most standard analog ICs leave something to be desired.

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You're looking for an edge. Through higher integration. Or performance improvements. Or unique packaging options. Things you've always wanted from standard analog products. But couldn't get.

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Utilizing our proven ASIC tool set and design methodologies, we can enhance your standard solution by changing the functionality or performance characteristics. Or by tightening electrical, environmental or unique quality specifications. Or simply by modifying your packaging to optimize your system's requirements. And give you working bipolar prototypes in as little as 6 weeks, CMOS in as little as 12. Consider the possibilities.

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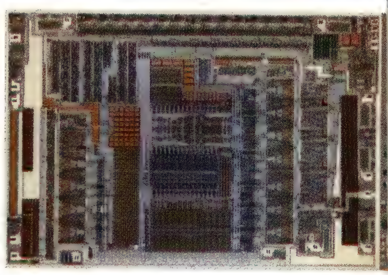
When one of our customers received a request from one of the major RBOCs to supply a telephone line equalizer with a very low group delay, we simulated the condition and simply re-wired the building blocks of one of our standard CMOS products. And delivered the goods, in less than 3 months.



standard: much more you need.

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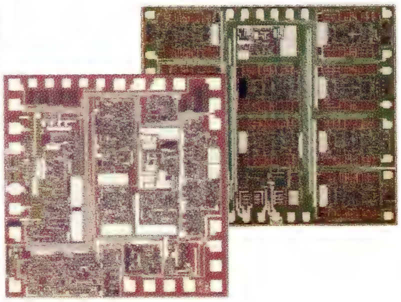
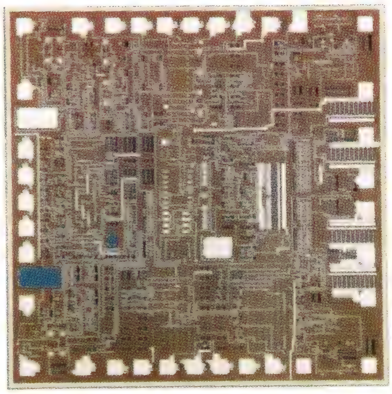
By quickly and easily adding a unique trim capability to one of our standard hard disk drive servo products, we delivered a much tighter voltage reference and satisfied a major customer's critical power fail detect requirement. On time. On budget. Giving him a real competitive advantage. Responding to a number of customers' immediate needs, we also solved a system yield problem through tighter pulse pairing. By adding trim capability to our standard ML 8464C pulse detector, we were able to raise the performance specs by 200% and quickly solve their application problem.



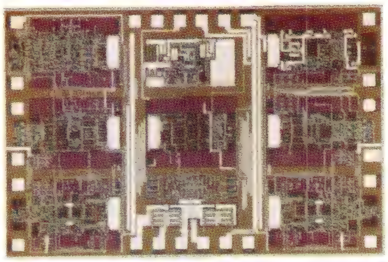
The Fewer, The Better.

When a major military supplier asked us to help solve a space problem on an advanced military radio, we used our FB 3490 tile array and existing macros to combine three 100KHz PWM controllers onto a single chip, in a single compact package. Quickly turning a standard answer into a small wonder.



The Smaller, The Better.

After evaluating our ML4621 Fiber Optic Inter-Repeater Link quantizer, three different networking companies asked us to develop smaller, lower power versions of our standard offering. The result? Two new versions, in TTL and ECL, each optimized for a particular interface, with lower pin counts and power consumption.



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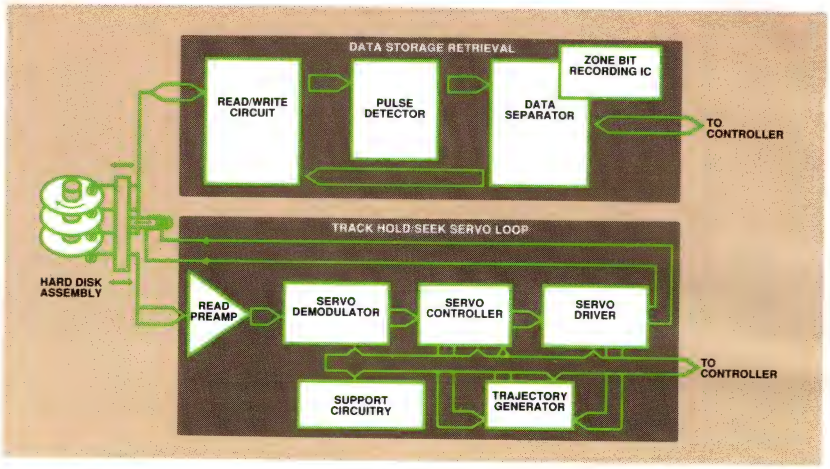
NOTES FOR DISK DRIVE DESIGNERS

How to design a strategic advantage into your next disk drive.

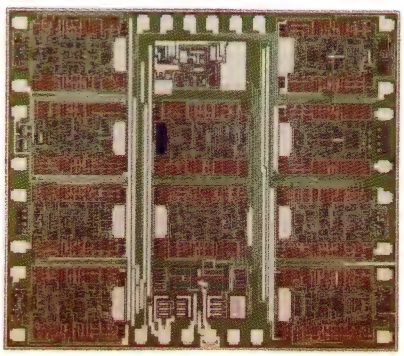


Micro Linear's full set of HDD ICs support both dedicated and embedded servo disk drives with read/write preamps, pulse detectors, phase locked oscillators and 8-bit data converters.

In the disk drive business, time to market is everything. Yet you can't be satisfied with standard read/write and servo control solutions.

What you need is semi-standard. Products with higher performance. Higher integration. Or increased functionality. That you can get in time to capitalize on narrow windows of opportunity. With a minimal amount of risk.

Semi-standard solutions like our ML8464C pulse detector, the first chip to offer a +/-1 nanosecond pulse pairing performance advantage, reducing bit error rates and increasing yields. Or our ML4041/4042 pulse detectors that combine 1 ns pulse pairing with 2 μs write-to-read recovery in the industry-standard footprint.



Semi-standard solutions like the ML4401 Servo Demodulator are based on Micro Linear's tile array technology, allowing modification of functional blocks to gain a competitive edge.

Or our ML4400 Chip Set that provides a highly integrated solution for fast-access, high TPI dedicated servo systems. It's a standard, off-the-shelf solution that's been designed with our bipolar tile-arrays. So you can start with our standard solution or modify the functional blocks to gain a competitive edge. And get working prototypes in as little as 6 weeks.

Got a high data rate drive that you want to race to market? Our new ML4025 data separator runs up to 33MB/s and is the only chip to support both RLL (1,7) and RLL (2,7) codes. Add constant density recording capability with our ML4417/4427 ZBR™ chip and you can achieve storage density advantages, with a VCO that operates over a 4:1 range up to 100 MHz.

You can even specify custom packaging options on any HDD product to satisfy critical on-board space requirements.

Want to know more about how you can gain a competitive advantage on your next drive? Just call (408) 433-5200, ext. 403, or write to:

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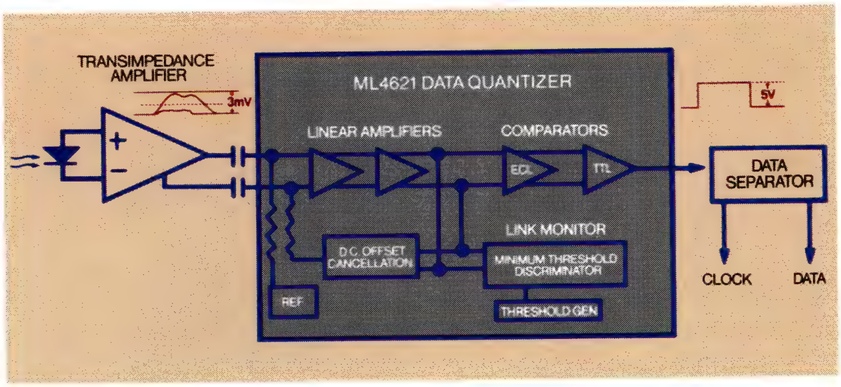
NOTES FOR ANALOG SYSTEMS DESIGNERS

Now there's a high performance single-chip solution for quantizing fiber optic signals.

Micro Linear's ML4621 is the first complete solution for converting low-level analog pulses from a fiber optic PIN diode preamp to digital signals, enabling you to interface with the clock recovery circuit.

The ML4621 is a highly integrated high performance solution for many different types of fiber optic receivers, including IEEE 802.3 and IEEE 802.5 Local Area Networks.



ML4621 converts Low Level Pulses from a PIN Diode Preamp into Clean Digital Signals.

High Frequency Design Made Easy

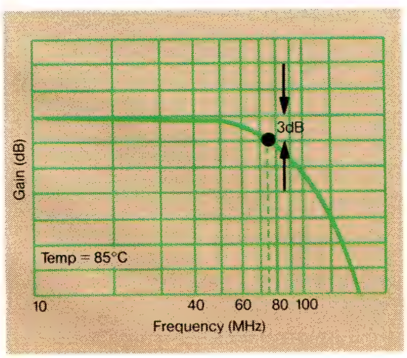
The ML4621 contains all the necessary circuitry for quantizing signals at data rates up to 100Mbaud. The chip includes a high speed comparator, wide band amplifier, a link monitor and a DC offset cancelling circuit. The high level of integration greatly simplifies the design of a fiber optic receiver by eliminating multiple discrete devices.

The ML4621 data quantizer can accept a wide dynamic range of signal strengths at its input, up to 55 dB.

The wide dynamic range means the ML4621 can be used where combinations of high and low voltage input levels might saturate less accommodating, discrete solutions. The quantizer's low noise voltage (25μV) makes it insignificant compared to other components.

Once your data signal has gone through two cascaded stages of wideband (50MHz) gain amplification, you can choose between either a single +5V TTL comparator, or a +5V or −5.2V ECL comparator to interface with other blocks.

For minimum use of board space, two other versions, the ML4622 and ML4623, are available in smaller packages. One has only TTL outputs and the other has only ECL outputs.



ML4621's Wide Bandwidth makes it usable to 100 MBaud

Built-In Link Monitor

A user adjustable link monitor prevents incorrect data from being passed by disabling data outputs when incoming signals fall below externally set threshold levels. The circuit also transmits a status signal to the system.

Semi-Standard Versions

The ML4621 family is developed on Micro Linear's family of bipolar tile arrays. It allows easy customization to your specific applications, including the addition of blocks, such as a Fiber Optic LED driver, or a transimpedance amplifier, or changes in I/O and other packaging options.

Call Or Write For More Information

If you would like more information on the ML4621 fiber optic data quantizer, or on Micro Linear's complete line of linear devices, call (408) 433-5200, extension 900. Or write:

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NOTES FOR POWER SUPPLY DESIGNERS

Now you have a choice for your power supply controller.

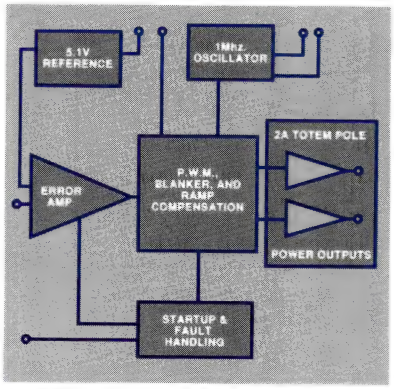
Standard devices for maximum performance.

1. Introducing three new single-chip Switch Mode Power Supply controllers that save space, money and time.

The new 16-pin ML4825 and ML4823 are improved pin-compatible replacements for the UC1825 and UC1823. A third new controller, the ML4809, is packed with extra features and functions for better stability, easier starting and synchronization.

PART TYPE	SOFT START RESET	UNDER-VOLTAGE OUTPUT STATE	COMPARATOR TO OUTPUT DELAY
ML4823 ML4825	COMPLETE	LOW	40 nS
UC1823 UC1825	PARTIAL	FLOAT	50 nS

Micro Linear/Unitrode Comparison



Micro Linear PWM Controllers Provide Maximum Performance

The ML4809 starts with all the features of the ML4825, then adds even more:

Synchronization:
- separate clock I/O pins
- wide dynamic range VCO
- toggle flip-flop output and preset inputs

Stability:
- on-chip programmable ramp compensation
- blanker to reject turn-on spike
- completely independent error ramp

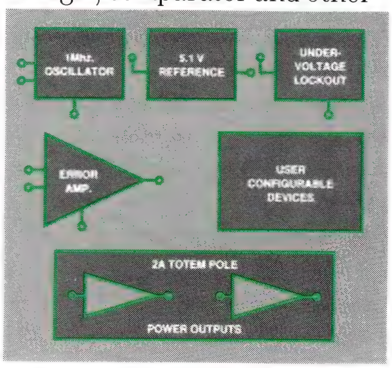
Start-up/Fault conditions:
- 7V hysteresis on under-voltage lockout
- full reset with programmable delay

If one of these new standard controllers doesn't meet your special high-frequency system needs, Micro Linear can provide a semi-standard part to your specific applications.

Semi-Standard devices for maximum flexibility.

2. Announcing the new FB3480, the first array specifically designed for high frequency Switch Mode Power Supply applications.

The FB3480 technology allows both Standard and Semi-Standard SMPS controllers to be quickly and easily developed starting from the same piece of silicon. This array contains crafted high performance "core cells" optimized to perform all the standard functions found in all PWM controllers. In addition a large area of uncommitted components on the chip can be configured to your specifications using Micro Linear's library of "soft macros." These macros implement a full complement of logic, comparator and other functions which make your controller unique. This approach allows you to evaluate the performance of the standard products then to customize a unique solution with a minimum of cost and effort, without sacrificing performance.



ML3480 Array Enables Easy Custom Design

For more information on the new single-chip standard and semi-standard SMPS controllers from Micro Linear, call (408) 433-5200, ext. 900.

Or write:
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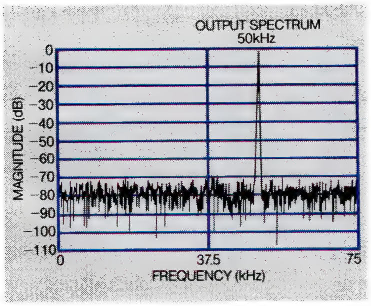
New 8-bit A/D converters with sample and hold maintain accuracy at 50KHz.

The new ML2258 and ML2281 series from Micro Linear maintain true 8-bit accuracy while digitizing a 0V to 5V, 50KHz sine wave. This gives you near ideal signal-to-noise of 47dB. All devices come with either a double buffered parallel or serial digital interface. Yet, these devices are superior for interfacing to temperature, pressure and position transducers due to low cost and ease of use.

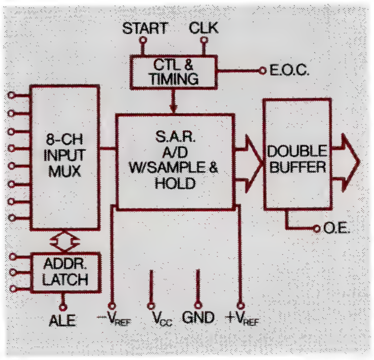
Dynamic Performance and 8-bit Guaranteed Accuracy

Dynamic performance and 6 microsecond conversion time make the ML2258 and ML2281 series ideal for signal processing as well as for digitizing sensors.



The FFT Plot of the ML2258 Converting a 50 KHz, 0 to 5V, Low Distortion Sine Wave Input.

Total unadjusted error in the ML2258 and ML2281 series is ±½ or ±1 LSB, which includes the sum of nonlinearity, full scale and zero scale errors. It is important to note that no full scale or zero adjust is required.



ML2258 Block Diagram

Designed for Ease of Use with a Choice of Analog Inputs

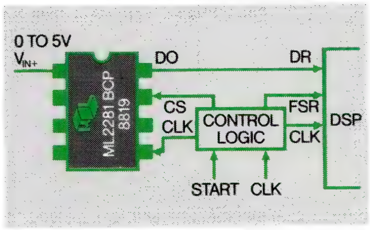
With all parameters guaranteed over the entire ambient temperature range, as well as ±10% tolerance of the single 5V power supply, the ML2258 and ML2281 series are designed for ease of use. Stable and repeatable conversions result from a digital code uncertainty of 1 mV.

Greater design flexibility is allowed by the 0V to 5V analog input range operating either ratiometrically or with a voltage reference up to 5V. The inputs are protected for up to 25mA maximum per input.

Power dissipation overall is extremely low—less than 3mA.

Digital inputs and outputs are both TTL and CMOS compatible.

The ML2258 microprocessor-compatible 8-bit A/D converter with 8 analog inputs has a double-buffered three state output and latched and decoded multiplexer address inputs. It is



ML2281 Serial DSP Interface

available in both 28-pin DIP or PCC.

The ML2281 series 8-bit serial I/O A/D converters provide a serial address of the 2, 4, or 8 analog inputs. ML2281 series DIP packages are 8, 14 or 20-pin configurations. In addition, the 8-input channel ML2288 is available in a 20-pin PCC. Prices start at only $2.95 each in 100 unit quantities.

Semi-Standard Options

Customized versions of both series of converters are available to incorporate alternate packages, different specifications or slightly modified functionality.

If you would like more information on the ML2258 or ML2281 series A/D converters, or on Micro Linear's complete range of linear devices, please call (408) 433-5200, extension 912, or write:

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Minimize parasitic problems in high-speed digital systems

Parasitics are usually small enough to have little effect on performance. However, the organizational, access-time, and coordinated-switching requirements of today's high-speed digital systems make ideal breeding grounds for these undesirable signals. Therefore, you must now account for those parasitics you could previously ignore.

James K Murashige, *Logic Devices Inc*

Parasitic problems, which are rarely overtly obvious, musn't be neglected in your system's design process. If they are, your system may be plagued with bugs, glitches, gremlins, and intermittent failures.

When digital designers encounter system problems, they frequently place the blame on the circuit ICs. However, IC manufacturers go to great lengths to characterize and test their devices. In most cases, it is not the ICs that are the main cause of parasitic problems. Rather, it is the pc-board interconnects between circuit components that prove problematic. Compounding the problem further is the fact that today's faster ICs are very susceptible to noise.

Parasitic problems due to pc-board-interconnect wiring are difficult to diagnose and cure because the parasitics are speed, layout, and material sensitive. It's possible to have thousands of interactions on a typical circuit board, and under certain conditions these interactions can combine to exceed digital noise margins and cause false triggering. Unchecked parasitics can also increase your circuit's power consumption, cause data loss, and cause devices to fail. By modeling the mechanics of parasitic operation early in the system-design phase, you can effectively anticipate and suppress problems.

In essence, electronic design involves the use of components to control, convert, and manipulate voltage and current to develop a useful function. Designers must therefore characterize electronic components in terms of how they interact with and relate to voltage and current. The defining relationships are resistance, capacitance, and inductance.

In the real world, no component is a pure resistance, capacitance, or inductance—all devices exhibit a mixture of R, C, and L. One of these components usually predominates; the others are considered parasitics. Wiring, whether discrete or printed, also contains R, C, and L components.

Resistance is the least troublesome parasitic because it has no dependence on speed. Even if the C and L quantities are quite small, parasitic capacitance and inductance cause a great many problems because they define a differential relationship between voltage and current.

The parasitic values of R, L, and C in circuit-board

In the real world, no component is a pure resistance, capacitance, or inductance—all devices exhibit a mixture of R, C, and L.

wiring are interrelated. A study of the makeup of resistive, capacitive, and inductive parasitics (**Fig 1**) makes it much easier to minimize their effects.

Copper-clad, glass-epoxy boards are typically used to achieve the desired high conductivity/low resistance qualities so important to wiring. Copper-foil thickness is customarily specified as the number of ounces of pure copper per square foot of board area. Each ounce contributes 0.00135 in. of thickness to the cladding. Parasitic resistance has a low value—a 10-mil-wide trace on a 2-oz copper-clad board has a resistivity of only 2.27 mΩ/linear in. Also, because resistivity is inversely proportional to the cross-sectional trace area, increasing cladding thickness or widening the trace proportionally lowers resistivity.

Parasitic capacitance arises because a circuit trace is one plate of a pc-board capacitor. Adjacent circuit traces, or inner layers of a multilayer board, are the other plates. The dielectric material for this parasitic capacitor is air and/or the board material itself. Dielectric constants vary for different board materials (it's about 5 for commonly used G10 epoxy boards). You can calculate board capacitance using the expression

$$C=KA/d,$$

where K equals dielectric constant, A equals the plate's surface area, and d equals the distance between the plates. Obviously, capacitance will be greatest over a large plate area with minimal plate separation. For example, a 10-mil-wide trace has a parasitic capacitance of 1.2 pF/linear in. of trace; the capacitance will double for a 20-mil-wide trace.

The self-induced magnetic field generated around a circuit trace carrying a current produces the parasitic inductance. Parasitic inductance is dependent on the length, width, and thickness of the trace as given by the expression

$$l=\text{length}/(\text{width}+\text{thickness}).$$

A 10-mil-wide trace will have an inductance of approximately 17.5 nH/in. Note that the above expression indicates that inductance will decrease as you increase either trace width or cladding thickness.

The simplified case of using a 10-mil-wide trace gives you some working values for R, C, and L, and also determines the qualitative effects of varying trace geometry. Though these parasitics have low values, they can become significant when you're working with high-speed signals. Digital-system designers should pay particular attention to the areas of power distribution and signal transmission.

Proper power distribution is critical

To operate at high speeds, ICs must, when switching, supply high levels of drive current on their outputs. Internal IC circuitry will draw more power when activated for full-speed operation. It is relatively simple to design a board's power-distribution system so that it satisfies steady-state conditions. However, parasitics in the system can cause momentary current limitations and supply-voltage drops. These transient conditions can show up in the signal outputs or couple through the power-distribution system to adjacent devices in the circuit.

To illustrate parasitic problems, consider the task of supplying power to an L7C185 8k × 8-bit static RAM (**Fig 2a**). Here, the L7C185 sits 6 in. away from an ideal 5V supply. V_{CC} is routed to the RAM along a

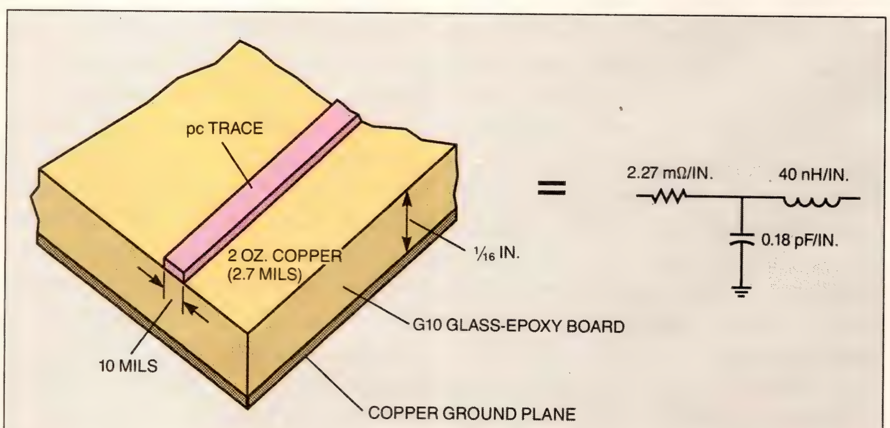


***Fig 1—You can minimize parasitic problems** by thinking of the pc board as a component. As the electrical-equivalent circuit illustrates, traces are really comprised of a combination of resistance, capacitance, and inductance.*

6-in.-long, 10-mil-wide trace, while a second 10-mil-wide, 6-in.-long trace provides the ground return. Each trace will have a parasitic resistance of 6×27 mΩ = 162 mΩ and an inductance of 6×17.5 nH = 105 nH. The L7C185 draws a quiescent current of 20 mA; for full-speed operation, it requires 160 mA.

Because a 160-mA current will introduce only a 26-mV drop in both the V_{CC} line and the ground return, the RAM's parasitic resistance will be negligible. The RAM's V_{CC} value will be 4.948V. However, parasitic trace inductance can cause problems because, as its defining equation $V = Ldi/dt$ illustrates, rapidly changing current through an inductor produces significant voltage drops. For example, a 20-nsec read operation from the L7C185 will generate an inductive voltage drop of 105 nH × 140 mA/20 nsec = 0.735V across both traces, leaving only 5 − 1.47 = 3.53V at the RAM's supply pin. Such a low value can lead to signal transients or cause data loss until V_{CC} can stabilize.

A more serious condition exists when the RAM powers back down and tries to stop the current flow. The sudden decrease in current generates a large negative voltage spike across the trace-inductive reactances relative to the power supply. For a 20-nsec off time, the chip's instantaneous voltage will be 5 + 1.47 = 6.47V. The result is the creation of signal transients that may overstress and damage the IC.

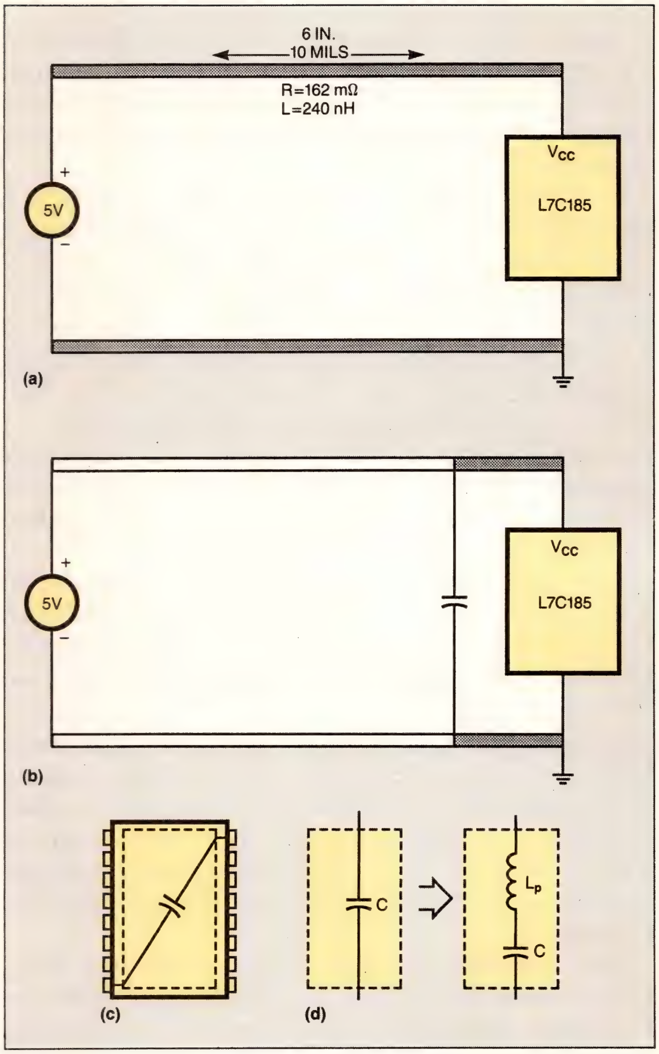


*Fig 2—**Proper decoupling techniques** can significantly reduce parasitic problems. The design goal here is to minimize the effects of parasitic inductance by keeping the I_{CC} current loop as short as possible.*

Good layout can make a difference

There are several solutions to the problem of parasitic inductance in power distribution, the most obvious being to widen the power traces. Widening power traces from 10 to 100 mils decreases inductance to 13.1 nH/in. In fact, the most effective board layouts employ multilayer boards, which have separate power and ground planes. In addition to providing the lowest possible inductance, this separate plane approach also simplifies the design of the power-distribution system.

The best solution to trace-inductance problems uses bypass capacitors to provide localized power sources for each IC. By physically locating decoupling capacitors next to each IC, you shorten the I_{CC} current loop to the physical length of the traces between capacitor and IC (**Fig 2b**). You can reduce trace length even more by using modern under-the-chip capacitors, which attach directly to the IC power pins—virtually reducing the trace length to zero (**Fig 2c**).

Before you can calculate minimum capacitor values, you must first establish an acceptable variation in the chip's supply voltage and then apply the defining equations for capacitance. Most modern ICs are specified to operate with a 5V ± 10% V_{CC}. While a 0.5V variation may be acceptable if you're considering only one IC, it may be too high when you consider the contributive effects of neighboring ICs switching at the same time. In memory systems, for example, simultaneous access to banks of eight or 16 devices is quite common. In this case, it is wise to hold the supply variation to 0.05V. Using the previous full-speed-operation figures of 140 mA and 20 nsec for current and switching time, respectively, the calculations yield a capacitance value of 0.056 μF.

By shortening the inductive trace length, decoupling

Digital-system designers should pay particular attention to power distribution and signal transmission.

capacitors also minimize overstress voltage by absorbing any inductive voltage spikes. In essence, you can think of decoupling capacitors as temporary current storage devices that help to smooth peak IC current demands.

Designers typically employ standard-value 0.1-μF capacitors for decoupling service. So why not use larger capacitors to reduce supply-voltage variations even further? There are a number of reasons, all of which are related to capacitor characteristics. The first has to do with size considerations—it's simply more difficult to physically place large capacitors close to ICs. Second, construction limitations increase the parasitic inductance in large capacitors. Large-value capacitors can have the equivalent inductance of several inches of circuit-board trace and negate the advantage gained by using larger capacitance values.

Finally, there's the problem of EMI. For maximum EMI suppression the decoupling capacitor must reach resonance in the frequency range of interest—typically 30 to 50 MHz. Again, larger-valued capacitors have intrinsically larger inductance values. Viewed from the standpoint of resonance, this larger inductance value lowers both the capacitor's resonant frequency and its EMI suppression effectiveness. Thus, smaller-valued capacitors with higher resonant frequencies suppress EMI much better. (Ceramic-type capacitors generally exhibit the best high-frequency characteristics for EMI suppression.)

The same interconnect parasitics that cause problems in power distribution also plague signal transmission, which is not surprising because power distribution and signal transmission are functional complements of each other. In power distribution, the signal source (power supply) remains constant while the load changes; in signal transmission, the signal source changes while the load stays the same.

The previous analysis of power-distribution parasitics used an empirical approach (a lumped parasitic circuit model) to solve the problem. The approach yielded good results and also simplified the explanation of the underlying principles involved. In signal transmission, however, the principal parasitic effects stem from the even distribution of parasitics along a line. Therefore, you must use a different approach to analyze the problem. Though this new approach involves a more involved circuit model, the analysis is applicable to power-distribution problems.

Because parasitic resistance is constant over frequency, it is generally not problematic. Parasitic capacitance and inductance, on the other hand, greatly affect signal transmission because of the time-derivative relationships they define between voltage and current.

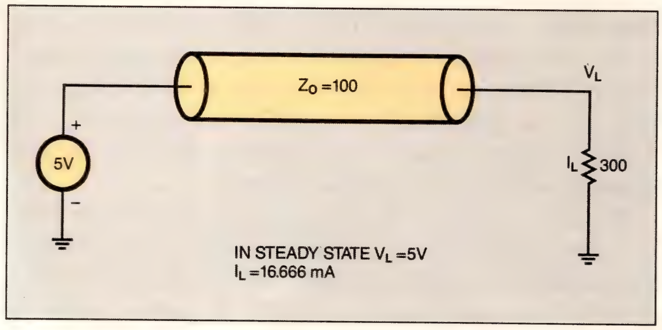


***Fig 3—You must match a line's characteristic impedance** at all interfaces if you want to minimize ringing, undershooting, or overshooting problems.*

One bad effect is delay. As a signal propagates down a trace it has to charge the distributed capacitors and inductors along the way, thereby introducing delay. System designers often neglect circuit-trace propagation delay when calculating worst-case delay paths. Instead, they focus on the source and driver specifications of the circuit's ICs. Unfortunately, trace-propagation delay can become a significant factor in high-speed systems that require large loads or critical timing requirements.

Assuming you have an ideal signal source, the propagation delay T_{PD} through a line will be equal to $\sqrt{LC}$. Returning to the 10-mil-wide trace example in **Fig 2A**, the delay per unit length calculates out to $T_{PD} = \sqrt{17.5\ \text{nH} \times 1.2\ \text{pF}} = 0.145$ nsec/in. The trace delay itself is small, but when it's combined with even moderate loading values it can create large signal delays.

When you're working with MOS circuitry, for example, loading is principally capacitive. You can evaluate the effect of this loading by applying the formula for T_{PD} to a calculated bulk value of C and L. Doing so, you obtain $T_{PD} = \sqrt{L(C_T + C_1)} = \sqrt{(LC_T) + (LC_1)}$, where C_T equals total trace capacitance and C_1 is the total capacitive load value. C_T is usually much smaller than C_1, so T_{PD} will be predominantly caused by the parasitic trace inductance combined with load capacitance—the LC_1 factor.

To illustrate delay problems, consider the design of a memory array utilizing a single source to drive eight L7C185 SRAMs (static RAMs) and in which similar signals (such as addresses) are daisy chained from one chip to the next. Each L7C185 presents a 5-pF load

on each input. With eight SRAMs in parallel, the total load capacitance equals 40 pF. If the circuit board is laid out well, the SRAMs will be located close to each other to keep trace lengths to a minimum.

Assuming that you can use a 6-in. length of 10-mil trace to connect all the RAMs, the trace contributes a capacitance value of 7.2 pF and an inductance of 105 nH to the delay calculation. Total T_{PD} then becomes $\sqrt{105 \times 7.2 + 40} = 2.23$ nsec. The example illustrates that trace inductance and IC load capacitance are indeed the major contributors to signal delay, with trace capacitance making only a minor contribution. It's obvious that, as with power distribution, propagation delay occurs because trace inductance retards the instantaneous flow of current. Therefore, the best way to minimize propagation delay is to minimize trace inductance by maximizing trace crosssectional area—by widening trace widths or paralleling trace runs.

Bring characteristic impedance into play

Because of the time-derivative properties of the distributed capacitance and inductance along the trace, voltage and current propagating down the trace maintain a fixed-phase relationship to each other. Given this fixed-phase relationship, you can use characteristic impedance, expressed by the relation $\sqrt{L/C}$, to model traces for signal-transmission analysis.

A second, more serious consequence of parasitic capacitance and inductance is the introduction of signal transients. These transients arise because of the reluctance of the distributed capacitance and inductance to allow instantaneous changes in voltage and current along the trace.

Signal transients—in the form of undershoot, overshoot, and ringing—can occur unless you match the characteristic impedance of a trace at its interfaces. Reflected voltage and current wavefronts generated to satisfy boundary conditions generate these transients, which can cause false switching, increase power dissipation, and generate EMI.

To illustrate the problem, consider the case of a 5V signal propagating down a 100Ω line terminated with a 300Ω load (**Fig 3**). Initially, a 50-mA current front (5V/100Ω) follows the voltage front as it propagates down the line. When the fronts reach the 300Ω load, a discontinuity develops—a 50-mA current is flowing through the line, but 5V into 300Ω equals only 16.7 mA. To satisfy this boundary condition, fronts of 2.5V and −25 mA reflect back down the line toward the signal source. The load voltage is now 5+2.5=7.5V

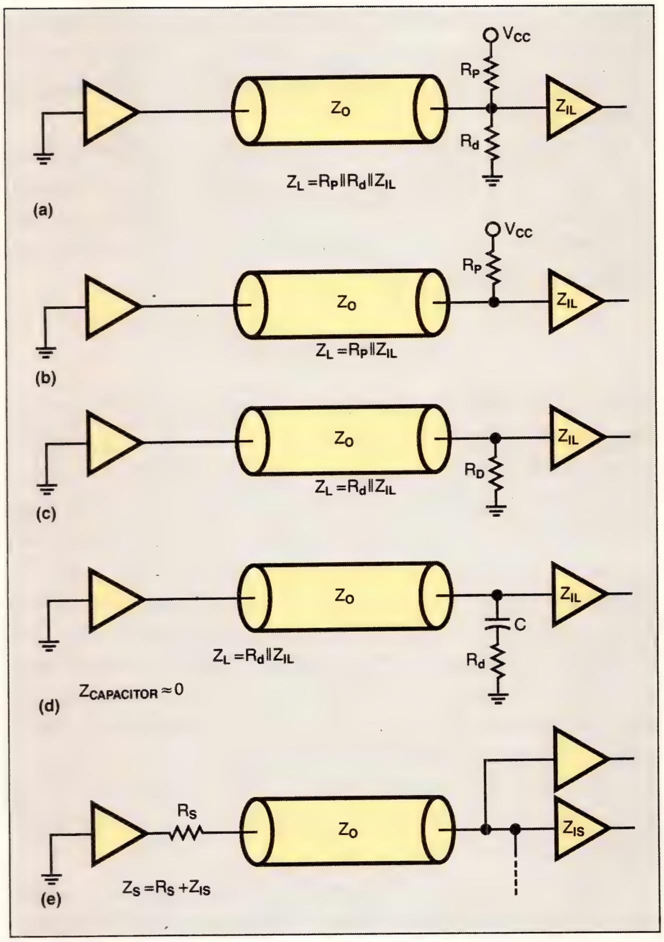


Fig 4—There are many impedance-matching techniques *available to solve transient problems. Though load-matching schemes **(a), (b), (c), (d)** are usually the preferred choice, you must turn to a source-matching scheme **(e)** when you're dealing with multiple loads.*

and current is 50−25 mA—values which satisfy the boundary conditions.

Back at the source, the reflected voltage and current fronts must again satisfy boundary conditions. Doing so may lead to more reflected waves. In time, the oscillations decay, and the line will achieve a steady-state condition of 5V throughout its entire length with a current flow of 16.6666 mA. A matching load of 100Ω would have satisfied boundary conditions and created no reflected waves.

Line reflections occur anytime signals are transmitted along unmatched lines. However, they only cause problems when they fail to coincide with the edge of the driven signal, a condition which arises when the signal rise time is faster than the period over which the reflections dampen out. To simplify reflection-mag-

The most effective solution to trace-inductance problems uses bypass capacitors to provide localized power sources for each IC.

nitude calculations, it's useful to define a reflection coefficient p where $V_{r(reflected)} = pV_{i(incident)}$. In general, you can derive p by satisfying boundary conditions as follows.

The voltage and current initially flowing through the line are V_i and V_i/R_o. At the boundary, the termination impedance, R_t, equals V_t/I_t. After reflection occurs, $V_t/I_t = R_t$. Given this relationship, you can calculate the reflection coefficient as

$$(R_t - R_o)/(R_o + R_t).$$

An examination of p yields several bits of information. If R_t is greater than R_o, positive voltage reflections will occur. Negative voltage relections occur when the opposite is true. For an open-circuited line, R_t dominates and $p = +1$. In this case, $V_r = V_i$ and the termination interface will generate a reflection of $2V_i$. High-impedance terminations such as this can possibly create overvoltage conditions and increase power consumption because of the higher voltage levels they generate. Sufficient overvoltage levels can damage the input of ICs or induce latchup in a CMOS device. With a short-circuited line, R_o dominates and $p = -1$. Therefore, $V_r = -V_i$, which negates V_i. Negative voltage reflections can cause false switching action when you're dealing with multiple signal edges.

When line and load impedances are matched, there are no transmission problems. Voltage reflections ping-pong along the line, attenuating themselves by p each time they reach the source or load. The reflections eventually decay to zero and the line achieves steady-state conditions. The decay time of the voltage reflections depends entirely on the reflection coefficients p at either end of the line and the amount of propagation delay down the line.

Choosing a suppression technique

You can suppress transmission-line transients by matching impedances at either the source or the load. Load matching is the best option because it allows you to minimize source impedance, which enhances drive capability and improves signal rise time and dc drive capability. Typically, the load will be the high-impedance input of a MOS IC, which means you'll have to lower load impedance to match the line impedance.

There are several ways to lower load impedance. One utilizes an active termination employing a pull-up/pull-down resistor network **(Fig 4a)**. The effective load impedance equals the parallel combination of R_P, R_D, and the output impedance of the IC. In addition to matching impedances, this technique also establishes an active termination voltage, which can be used to help a weak source driver with rise-time and fall-time performance. The matching technique does have one drawback, however: there's a dc current constantly being dissipated through the termination resistors.

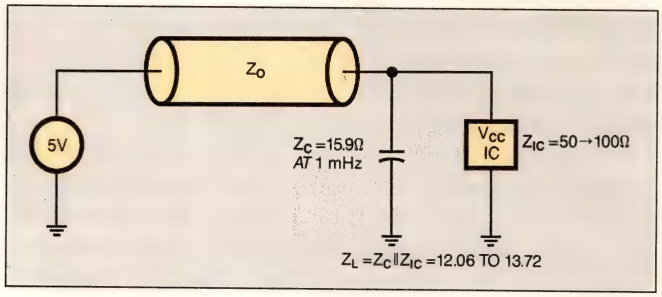


Fig 5—Transient problems in power-distribution systems *are significantly reduced when you use decoupling capacitors to minimize load-impedance variations.*

A second load-matching approach uses just a pull-up **(Fig 4b)**, or pull-down resistor **(Fig 4c)**. Either of these schemes solves the dissipation problem, but weaker source drivers will have problems with the additional load imposition, especially if multiple load paths are involved.

You can avoid all dc loading problems by using an ac-coupled load-termination scheme **(Fig 4d)**. During the switching phase, the capacitor is virtually transparent, and the pull-down-resistor impedance combines in parallel with the load impedance to match the line impedance. Under steady-state conditions, the capacitor blocks any current flow and removes the resistive load from the circuit. You choose the capacitor value to achieve a minimum impedance at the voltage-reflection frequency $V_{VR} = 1/2T_{PD}$.

To this point we've considered only a single impedance discontinuity at the load. In a typical system, however, discontinuities may occur anywhere there is a physical change in the transmission path. Such changes occur when you split a trace to drive multiple IC inputs, widen or narrow a trace, or pass through a connector.

With several discontinuities in each line or with multiple load locations, it may become impractical to match all load impedances. If so, you must opt for source-impedance matching. Typically, the signal source employs a low-impedance driver, so you must raise the network's source impedance to match that of the line. To raise the source-output impedance you simply add

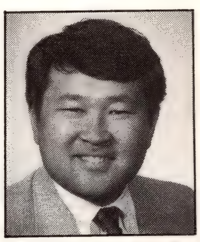
a series resistor at the driver output (**Fig 4e**).

Again, power distribution and signal transmission are complements of each other. You can see the relationship by applying the impedance-analysis techniques to power distribution (**Fig 5**). As the figure shows, the power-supply voltage remains constant while the impedance of the load varies. Voltage reflections and fluctuations occur during the transition between steady-state conditions. In order to minimize transients, therefore, you must minimize the factors that cause fluctuations from a steady-state condition.

Load impedance is the variable factor in power distribution, so your goal is to minimize load variations. Adding decoupling capacitors minimizes impedance variations because the capacitors become the dominant factor in the load-impedance equation. For example, assume that an IC being powered by the 5V power supply varies its current consumption from 50 to 100 mA. Correspondingly, the IC's output impedance varies from 100 to 50Ω—a 100% variation. At 1 MHz, a 0.01-μF decoupling capacitor has an impedance of 15.9Ω. When you consider the parallel combination of capacitive and IC impedances, the load will now vary from 12.06 to 13.72Ω—a 13.8% variation—which will lead to significant reductions in voltage transients.

EDN

Author's biography



James K Murashige is responsible for new product planning and application at Logic Devices Inc (Sunnyvale, CA). As such, he is involved in the development of high-speed DSP logic circuits, static RAMs, and SCSI controllers. James holds a BSEE degree from Johns Hopkins University (Baltimore, MD). In his off hours, he enjoys bicycling, hiking, gardening, and woodworking.

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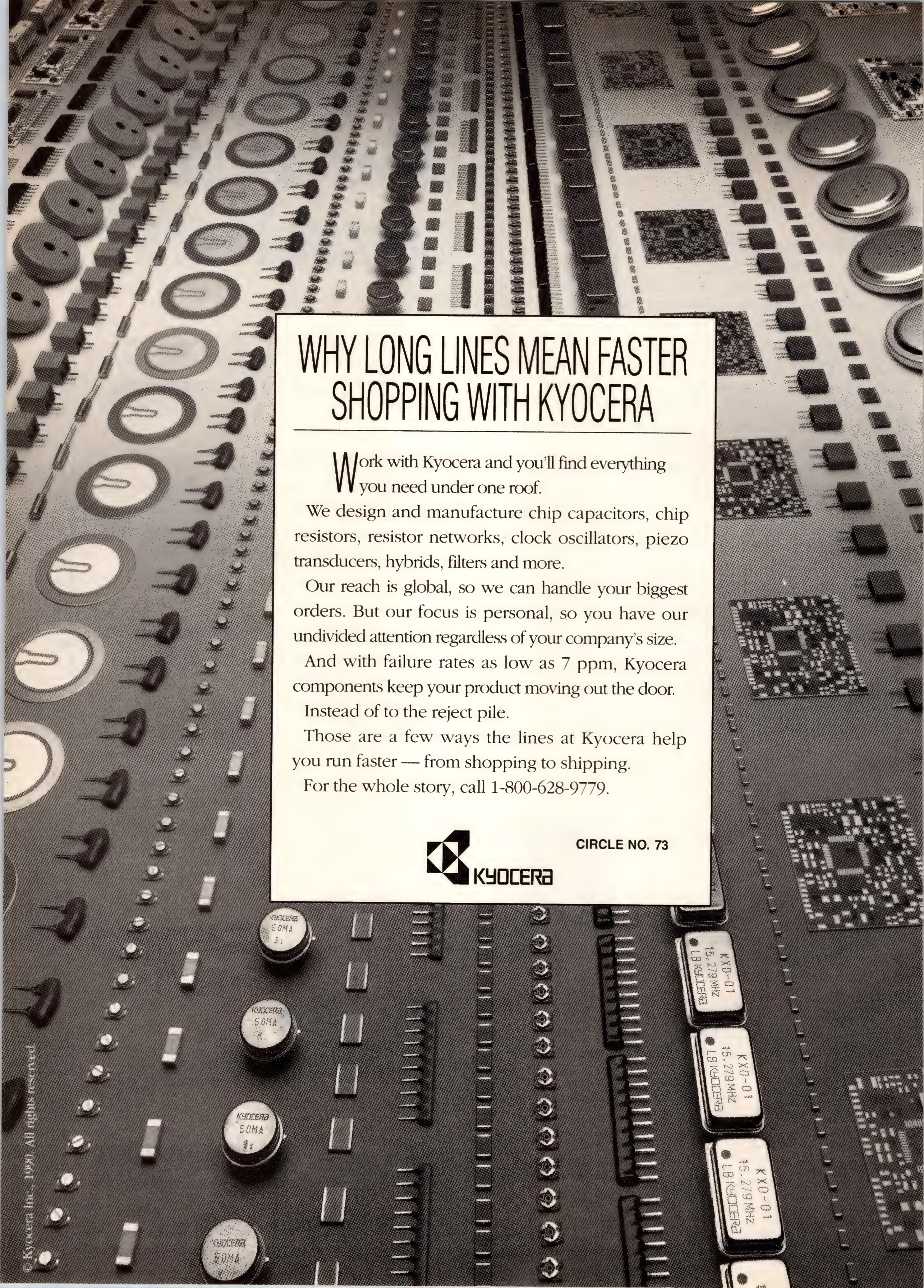

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Optimize code for vector/parallel computers

Despite advances in vector/parallel-processor throughput, you should still carefully analyze your program to identify potential areas for improvement. By following a defined plan, you can optimize your unmodified code with a minimum of effort. Then you can make minor changes to the source code to further improve throughput.

Howard W Page, Paul C Norris Jr, and Gary Brooks, *Convex Computers*

You can significantly increase the speed of many computer programs by rewriting the code with the target computer's architecture in mind. However, you may be unable or unwilling to do so if you're unfamiliar with the internals of the code. The following optimization method, which makes use of a profiler, will ensure that your code runs optimally on a vector/parallel supercomputer such as a Cray or a Convex without requiring that you change the source code. Profilers provide routine-level or loop-level execution profiles. A routine-level profiler is standard with Unix BSD4.2. After using this method, you might achieve even faster throughput by finding and optimizing some common programming oversights in the source code.

The first step to optimizing your code without changing it is compiling the program without any vectorization or parallelization. Then use the profiler to obtain a scalar runtime profile. This profile is a table of subroutines that lists the percentage of the total runtime the program spends in each subroutine, the number of seconds of CPU time for each subroutine, the number of times the program calls each subroutine, and the number of milliseconds per subroutine call. **Table 1** is an example of such a profile.

Note that the fspher and furim routines account for more than 93% of the total runtime. Therefore, optimizing these two routines would give the greatest benefit for the least effort. Getting fspher to go one-and-a-half times faster would result in a 23% speed increase, whereas getting lambda to go four times as fast would only result in a 1% speed increase.

After getting a runtime profile of the unoptimized scalar code, compile the program with vectorization turned on. Vectorization results in single instructions operating on multiple data elements. Another process, parallelization, results in multiple instructions working on multiple data elements simultaneously. You can vectorize in one of two ways: (1) vectorize only those routines high in the profile or (2) vectorize everything. Vectorizing only routines high in the profile involves fewer comparisons; vectorizing everything generally leads to slightly faster code. In either case, the goal is to compare the scalar and vector runtimes for each routine. After vectorizing the program, profile the vectorized compiled code. **Table 2** shows the profile for

To find where your code could most benefit from optimization, compile it with and without vectorization and compare the run-time profiles.

this same code with all subroutines vectorized.

Note that vectorization increased the speed of the first three routines—furim runs in one seventh the time, fspher runs in a little less than half the time, and lambda runs in almost one fifth the time. Note, too, that some of the less-often-run routines actually run slower after vectorization.

The lengthening of these routines is usually due to short vector lengths in loops. When the compiler can't discern the loop length, it vectorizes short loops. Because the compiler might vectorize some of these loops, you should be selective in choosing which subroutines to vectorize. Although vectorization yields some impressive speed increases, the overhead for vectorizing short loops can cause these loops to use more CPU time than they would have used as scalars.

For very short loops, the overhead that the vector registers use can swamp any gain you might realize from using vector registers rather than scalar registers. The parallel-processing overhead is usually at least an order of magnitude greater than that for vectorization. Therefore, it's imperative that you gather loop-length statistics.

Two other techniques for generating optimal unmodified code are also worthy of your consideration. One is subroutine in-lining, which is replacing a subroutine or function call in a parent routine with the actual code from the called routine. Some Fortran compilers in-line code automatically. There are two reasons for in-lining.

The first reason is to eliminate the overhead of calling a routine. The overhead for a subroutine call is computer-dependent. On a Convex computer, this overhead is on the order of tens of microseconds. Two general guidelines will help you determine whether eliminating this overhead would yield a noticeable increase in speed on a benchmark. On a Convex computer, the subroutine mcount gathers profiling statistics. To justify in-lining, mcount should take up more than 10% of the total CPU time. Also, the number of calls to an in-lining candidate should be at least in the hundreds of thousands for code that runs in a few minutes. Both the total time and the number of calls are indications of the CPU spending lots of time branching to subroutines. In the previous profiling example, the number of subroutine calls is too small for in-lining to be effective.

Theory and practice disagree

The second reason for in-lining is that it affords you the opportunity to increase optimization in the parent routine after you pull the child routine's code in-line. Programming theory suggests that when the program calls the child routine inside a loop, the loop has a chance to vectorize or parallelize. But subroutine or function calls inside the loop generally prevent automatic vectorization and parallelization.

In practice, in-lining rarely yields impressive speed increases because subroutines often have complicated structures. At best, you could increase the speed of a subroutine by a factor of two. Contrast this increase with the 4- to 8-fold increases from vectorization. Also, because most subroutines employ nested loops, code that consists of a loop with a subroutine call in it can seldom vectorize after in-lining. On the other hand, vectorizing can occur in highly modularized code.

A small DO loop such as

```
DO I=1,4
  A(I) = 0.0
END DO
```

runs faster on most supercomputers with scalar optimi-

Table 1— Profile of unvectorized code

Subroutine name	Percent time spent in subroutine	Time spent in subroutine (sec)	Cumulative time (sec)	Number of subroutine calls	Time/call (msec)
furim	69.5	164.07	164.07	100	1640.71
fspher	24.4	57.50	221.57	100	575.00
lambda	4.5	10.66	232.23	301	35.42
cvtmot	0.5	1.24	233.47	100	12.40
molvir	0.2	0.49	233.96	100	4.90
mcount	0.2	0.36	234.32		
tabx6	0.1	0.35	234.67	1	350.00

Table 2 — Profile of vectorized code

Subroutine name	Percent time spent in subroutine	Time spent in subroutine (sec)	Cumulative time (sec)	Number of subroutine calls	Time/call (msec)
furim	44.6	24.45	24.45	100	244.50
fspher	42.5	23.31	47.76	100	233.10
lambda	4.1	2.25	50.01	301	7.48
cvtmot	3.0	1.63	51.64	100	16.30
mcount	1.2	0.65	52.29		
molvir	1.0	0.56	52.85	100	5.60

zation than with vector or parallel optimization. Another way to generate optimal unmodified code is loop unrolling, which can speed the scalar loop a bit more. When unrolled, the DO loop becomes

```
A(1) = 0.0
A(2) = 0.0
A(3) = 0.0
A(4) = 0.0
```

Loop unrolling eliminates the overhead associated with incrementing the loop index or deciding when to terminate the loop (executing a test and branch).

For fixed-length loops, the supercomputer's scalar/vector crossover point determines whether to run the code in scalar, vector, or parallel mode. If the loop length changes while the program is running or if a loop has a low minimum and high maximum range, you must use a method called dynamic runtime selection. This DO loop,

```
DO I=1,N
  A(I) = 0.0
END DO
```

has the following equivalent dynamic runtime-selection code:

```
      IF (N .LE. Q) THEN
c where Q is equal to the computer's scalar/vector
c crossover
c Scalar directive forces loop to run scalar
C$DIR SCALAR
          DO I=1,N
             A(I) = 0.0
          END DO
      ELSE
c Go ahead and vectorize this loop
          DO I=1,N
             A(I) = 0.0
          END DO
      END IF
```

Some compilers can unroll loops and create dynamic selection code. These compilers let you generate code without modifying the source.

Short loops need special attention because of the overhead that vectorization and parallelization add to these loops. To determine which loops are short, use a loop-level profiler. This tool will tell you (1) the length of each loop, (2) how much time is spent executing each loop, and (3) how many times the loop is executed. When profiling loops, remember the law of diminishing returns—concentrate on loops in routines that are high on the routine profile.

Unfortunately, loop-level profilers are not always available for vector/parallel computers. Therefore, you may have to write and insert profiling code yourself. The following code is shown before and after inserting profiling and debugging statements, or instrumentation.

```
      SUBROUTINE TEST
     &(GRP,ROW,Q,X,AVER,COV)
      INTEGER GRP, ROW
      REAL Q(100,100), COV(6,6,100), X(100,100,6),
     &AVER(6,100)
      DO 200 GRP=1,100
      DO 100 ROW=1,100
      Q(ROW,GRP)=COV(1,1,GRP)*
     &(X(ROW,COL,1)-2.0*AVER(1,GRP))
100   CONTINUE
200   CONTINUE
      RETURN
      END
```

The instrumented code:

```
      SUBROUTINE TEST
     &(GRP,ROW,Q,X,AVER,COV)
CONVEX SHOWTIME ...
         COMMON / _TIME_ / _TIMES_ ,
     & _COUNTS_
c cputime is cpu timer with microsec accuracy
         REAL*4 _TIMES_(999) , CPUTIME
     & _TEMPTIME_
         INTEGER*4 _COUNTS_(0:128,999) ,
     & _I1_ , _I2_ , _I3_
         INTEGER*4 _LEN_
CONVEX SHOWTIME ...
      INTEGER GRP, ROW
      REAL Q(100,100), COV(6,6,100), X(100,100,6),
     &AVER(6,100)
      DO 200 GRP=1,100
CONVEX SHOWTIME ...
         _I1_ = 1
         _I2_ = 100
         _I3_ = 1
         _LEN_ = ( ( _I2_ - _I1_ ) / _I3_ ) + 1
         _LEN_ = MIN( _LEN_ , 128 )
```

In-lining subroutines is not as effective as you might expect because the routines often have complicated structures.

```
       _LEN_ = MAX( _LEN_ , 0 )
       _COUNTS_( _LEN_ , 1 ) = _COUNTS_
    &  ( _LEN_ , 1 ) + 1
       _TEMPTIME_ = CPUTIME(0.0)
      DO 100 ROW=1,100
      Q(ROW,GRP)=COV(1,1,GRP)*(X(ROW,COL,1)
    &-2.0*AVER(1,GRP))
100   CONTINUE
CONVEX SHOWTIME ...
       _TIMES_( 1)= _TIMES_( 1) +
    &CPUTIME(_TEMPTIME_)
200   CONTINUE
      RETURN
      END
```

The loop-level profiler gathers timing information each time the program calls a subroutine and places cumulative times in a common block. Periodically, the profiler writes this common block out to a file. Rather than running long programs to completion, you may want to stop the code when you're sure the profile will not change significantly by letting the code run further. By cutting the runtime, you can examine a job that would normally take hours of CPU time after a few minutes. You can also determine which loops in a given subroutine take up a lot of CPU time.

Unfortunately, this approach is intrusive. The compiler can't interchange the GRP and ROW loops in the instrumented code due to calls to the timing routines. Use a tool that runs at either the assembler or compiler level to instrument your code nonintrusively. Convex's CXpa is such a tool.

After vectorizing, performing dynamic selection, and loop unrolling, you've done all you can to ensure that your unmodified code is running optimally in vector mode.

EAP isn't automatic

The next step is tuning your code for parallel performance. Typically, vector/parallel compilers only perform efficient automatic parallelization (EAP) in two instances. First, for loops of sufficient length (on a Convex computer, more than 256-elements long), the compiler can strip-mine the code in parallel. Thus, the computer executes vector strips on separate heads. This process is called loop spreading. Alternatively, nested loops that contain no loop-carried dependencies (that is, each iteration is independent of all others) will have the outermost loop parallelized and the innermost loop vectorized. This process is called concurrent outer, vector inner.

If the computationally intensive portions of your code satisfy one or both of the loop-spreading or concurrent-outer-vector-inner conditions, you can compile your code with vectorization and parallelization and obtain optimal unmodified parallel code. In other cases, however, you might have to closely examine the source code and possibly make some changes.

Program tuning for a parallel system is simply an extension of the scheme that you use for vectorization. Use a loop-level profiler to identify loops that are long enough to run in parallel, then adjust the optimizations accordingly. A good parallelizing compiler will generate code that balances the computational load between all the CPUs in a computer at runtime. For example, if there is a loop of length 200 in a program, a naive parallelization scheme would produce a vector of length 128 for one processor and $200-128=72$ for the other. This parallelization would yield unbalanced results on a 2-processor system, and a 4-processor system would offer no additional benefits. Load-balancing for a loop of length 200 would result in two vectors of length 100 on a 2-CPU system and four vectors of length 50 on a 4-processor system.

Further tuning involves placing directives on the various loops that can potentially run in parallel. For example, a Convex compiler has a directive to force a loop to run in vector, but not parallel, form. The compiler uses this directive if a loop is long enough for vector processing but not for parallel processing. Directives control vector and parallel strip-mine lengths. A directive even specifies at which three points to cross over from scalar to parallel processing, parallel to vector processing, and vector to concurrent vector processing.

Other techniques can also increase your code throughput. Many of the following tricks have been culled from tuning hundreds of benchmarks. And although these methods require code modification, the changes are minimal and let you greatly improve code efficiency.

One common class of problems—with an easy solution—is memory-bank conflicts. These conflicts arise because Fortran data arrays are stored in column-major order with the first index varying most quickly. When accessing data by the second or higher index, you must know how the array is allocated in memory. A supercomputer's memory typically comprises a number of banks. Each bank has a cycle time of, for example, eight clock cycles. Once a computer reads a word from a bank, that bank is busy and the computer can't read from that bank again until eight cycles later. If

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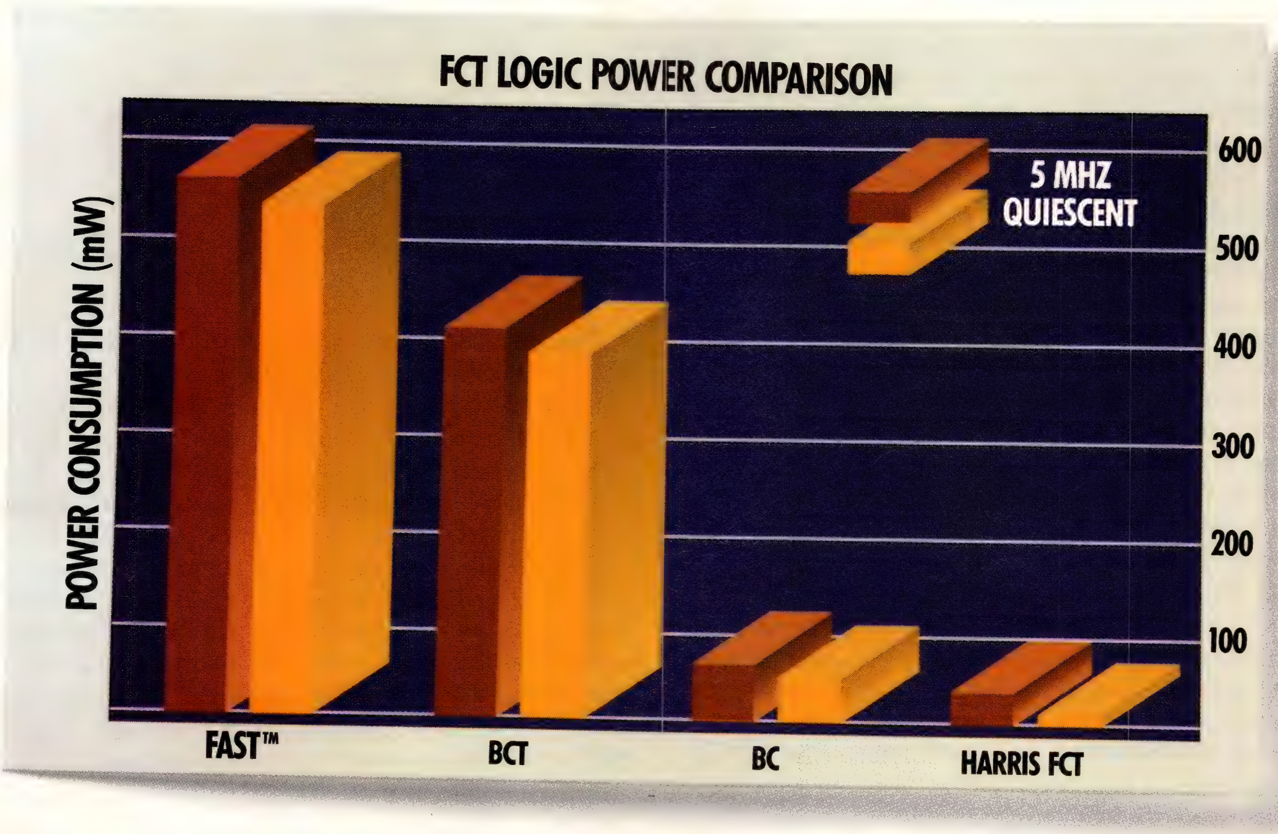

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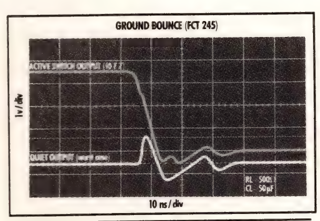

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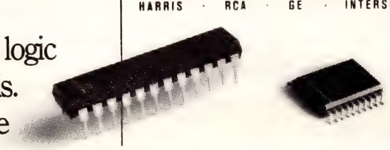


Making your DIMENSION statements ODD can often solve memory-bank conflicts and speed throughput.

the leading dimension of an array is not relatively prime to the number of memory banks, or the interleaving factor, and the second index accesses data, memory-bank conflicts will occur. Since interleaving factors are almost always powers of two, you will usually avoid bank conflicts if you make sure the leading indices in the DIMENSION statement are ODD.

For example, if your code has an array dimensioned as A(100,50) and your algorithm accesses A by row, then changing the dimension of A to A(101,50) will increase your code's throughput. You can get the same effect by reversing the dimensions to A(50,100), but implementing this reversal would require more work. Some compilers have row-wise directives, which transparently force an array to be stored in memory in row-major rather than column-major order.

Another way to improve your code's throughput is through matrix inversion. Many codes have comment lines that reference the generation of a variable's inverse to calculate the solution of a system of equations. But factoring the matrix and solving a set of equations is often faster than computing the inverse directly and performing a matrix-vector multiply. Most systems provide special library routines for factoring and solving systems of equations. Using these library routines assures you of getting optimal performance out of your system.

The DO-IF interchange of invariant-IF statements may also provide an opportunity to optimize your code. An invariant-IF statement is one in which the result depends on a value, K, that doesn't change inside the loop. An example of an invariant-IF test is

```
DO I = 1, N
  IF(K.EQ.0) THEN
    A(I) = 0
  ELSE
    A(I) = 1
  END IF
END DO
```

Note that the test yields the same result regardless of the value of I.

Most compilers can fully vectorize this code, and the compiler messages could easily dupe unsuspecting users into concluding that their code is running quickly. However, by moving the invariant-IF test outside the DO loop, the slower conditional statement executes only once.

```
IF(K.EQ.0) THEN
  DO I = 1, N
    A(I) = 0
  END DO
ELSE
  DO I = 1, N
    A(I) = 1
  END DO
END IF
```

The same idea works with boundary conditions. The IF test is of the form IF(I.EQ.1) or IF(I.EQ.N). Once you restructure the code to separate the loop into one or two pieces for the boundary condition and one for the inner points, the code runs much faster. These changes also increase the code's speed on serial processors.

Transformations that involve redundant subroutine calls at the DO-CALL interchange are a bit tricky. Due to the compiler promoting parameters to vectors across that interchange and the resulting bookkeeping difficulties, these transformations can take more than a bit of typing and debugging. When the main program calls a subroutine within a loop and in-lining the subroutine doesn't yield additional vectorization (usually due to DO loops within the subroutine), you can realize substantial performance gains. These gains result from pushing the DO loop into the subroutine and doing additional loop distribution. For example,

```
DO I = 1, N
  CALL TEST(A,B,C)
END DO
```

becomes

```
CALL TEST(A,B,C,N)
```

Subroutine TEST will look something like

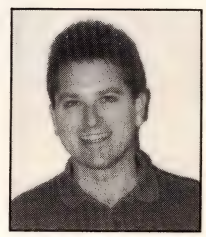
```
SUBROUTINE TEST(A,B,C,N)
DO I = 1, N
.......
END DO
```

This transformation usually involves promoting numerous scalar variables to dimensioned variables. You should practice patience and use a source-code revision-control system of some sort when attempting it.

These transformations often yield impressive performance improvements in vector processing, but you must use the exact opposite approach for parallelizing code. The reason is that you want to get at the innermost set of calculations for vectorization but need to see the "big picture" for parallelization. Unfortunately, Fortran and C parallel compilers generally miss the big picture since they don't perform interprocedural analysis.

Ideally, if a program calls a subroutine 1000 times, you'd break your code into 1000 pieces and run each piece in parallel on separate processors. This process is called macrotasking. In contrast, once you start microtasking your program (parallelizing at the loop level), you reduce the amount of parallel benefit available to your program. Until interprocedural analysis becomes standard in Fortran and C compilers, it's up to you to look for large bits of code with parallel potential. To run a subroutine in parallel, you must make sure all local variables in the subroutine are separate for each processor. Usually, you can do so by making the subroutine re-entrant. Further, you can inform the compiler, usually via directive, that it can process the subroutine in question in parallel with other subroutines or tasks. EDN

Authors' biographies



Howard W Page has been with Convex (Dallas, TX) for four years as a mathematical software specialist. His primary responsibilities include analyzing performance benchmarks. Howard earned a BS in math from Guilford College (Greensboro, NC) and an MA in applied math from the University of Maryland.

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Gary Brooks is a software engineer at Convex. He has a BS in computer engineering and an MS in computer science from the University of Illinois. At Convex, Gary designs and implements development tools.

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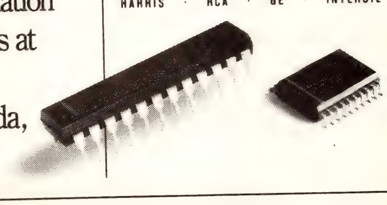

CIRCLE NO. 76

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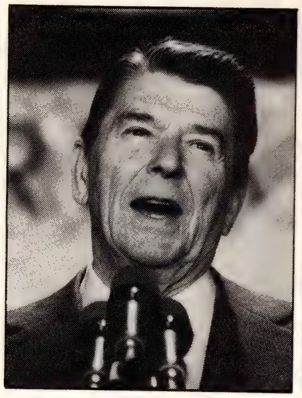
In 1980, Ronald Reagan is elected President of the United States…



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In 1981, Sandra Day O'Connor is the 1st woman on the Supreme Court…

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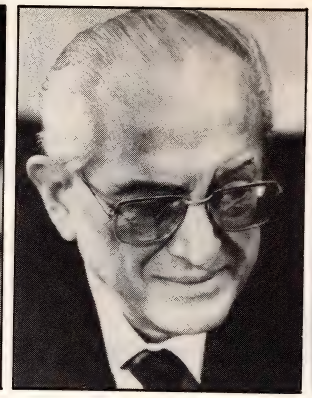
In 1982, Yuri Andropov is elected as the leader of the USSR…



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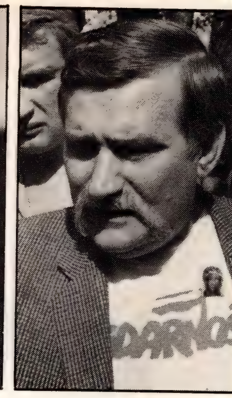
In 1983 Lech Walesa Poland wins the Nob Peace Prize…



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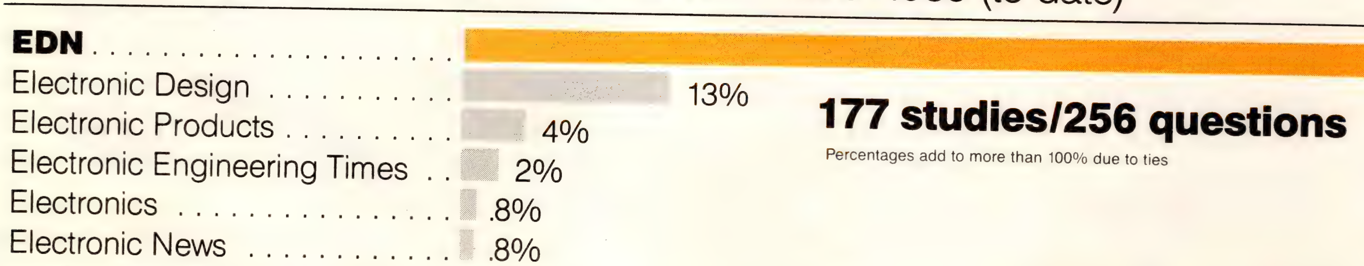

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*Independent studies are conducted across customer/prospects lists or TIDS lists, not across a magazine's or newspaper's own list, which results in obvious bias. **Results based on the question

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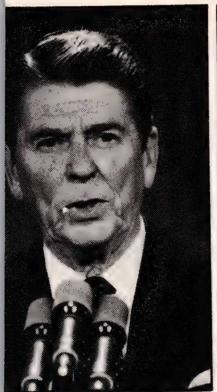

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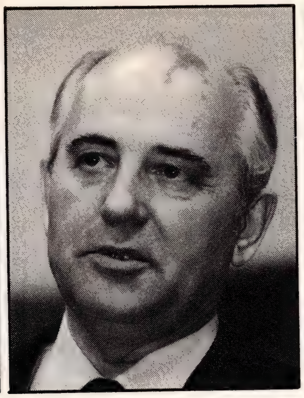
In 1985, Mikhail Gorbachev is elected as the leader of the USSR...



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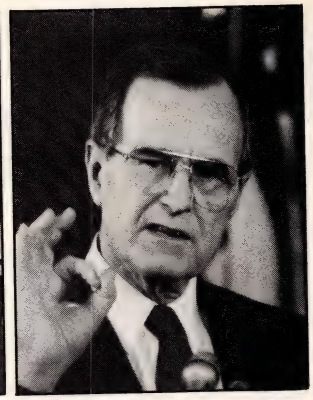

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3	2	4	5

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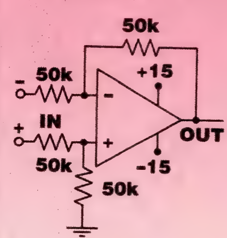
ERROR TERMS (μV)					
Vos MAX	50	100	90	60	75
Ios MAX x 25kΩ	6	70	50	70	4
MIN Gain 10V out	14	5	3	5	50
MIN CMRR ±25V in	22	20	13	22	39
MIN PSRR Vs = ±15V ±10%	6	9	9	9	9
SUM OF ALL ERROR TERMS (μV)	**98**	**204**	**165**	**166**	**177**
0.1Hz to 10Hz NOISE (μVp-p)					
Voltage Noise	0.50	0.38	0.23	0.38	0.50
Current Noise x 50kΩ	0.11	0.75	0.70	0.75	0.10
Resistor Noise	0.55	0.55	0.55	0.55	0.55
RMS SUM (μVp-p)	**0.75**	**1.00**	**0.92**	**1.00**	**0.75**
DRIFT WITH TEMP (μV/°C)					
MAX TCVos	1.0	1.2	1.0	1.2	2.0
MAX TCIos x 25kΩ	0.1	2.1	1.0	2.1	0.2
SUM OF DRIFT TERMS (μV/°C)	**1.1**	**3.3**	**2.0**	**3.3**	**2.2**
MAX SUPPLY CURRENT (μA)	**560**	**2000**	**3000**	**2000**	**600**
PRICE, Thousands	97¢	MORE	MORE	SAME	MUCH MORE



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CIRCLE NO. 77

DESIGN IDEAS

EDITED BY ANNE WATSON SWAGER

Meter quickly measures low-speed rpm

David Sherman
David Sherman Engineering, Everett, WA

The tachometry circuit in **Fig 1** accurately measures rotating machinery's surface speed in one revolution by taking the reciprocal of the period. The circuit produces an analog voltage that directly corresponds to the surface speed of a rotating drum or disk in ips. If you add the appropriate scale factor, the circuit will yield an output proportional to rpm.

The circuit's component values allow it to measure the rotation of a 6-in.-diameter drum with a single optointerrupter hole. The drum rotates anywhere from 3.2 to 320 rpm, which equals a surface speed of 1 to 100 ips. The circuit's corresponding output voltage ranges from 0.1 to 10V.

You must attach a pulse source, such as the optointerrupter formed by D_1 and R_1, to the machinery. This source should generate a pulse for each revolution. Q_1 drives a timing network, which generates a pair of

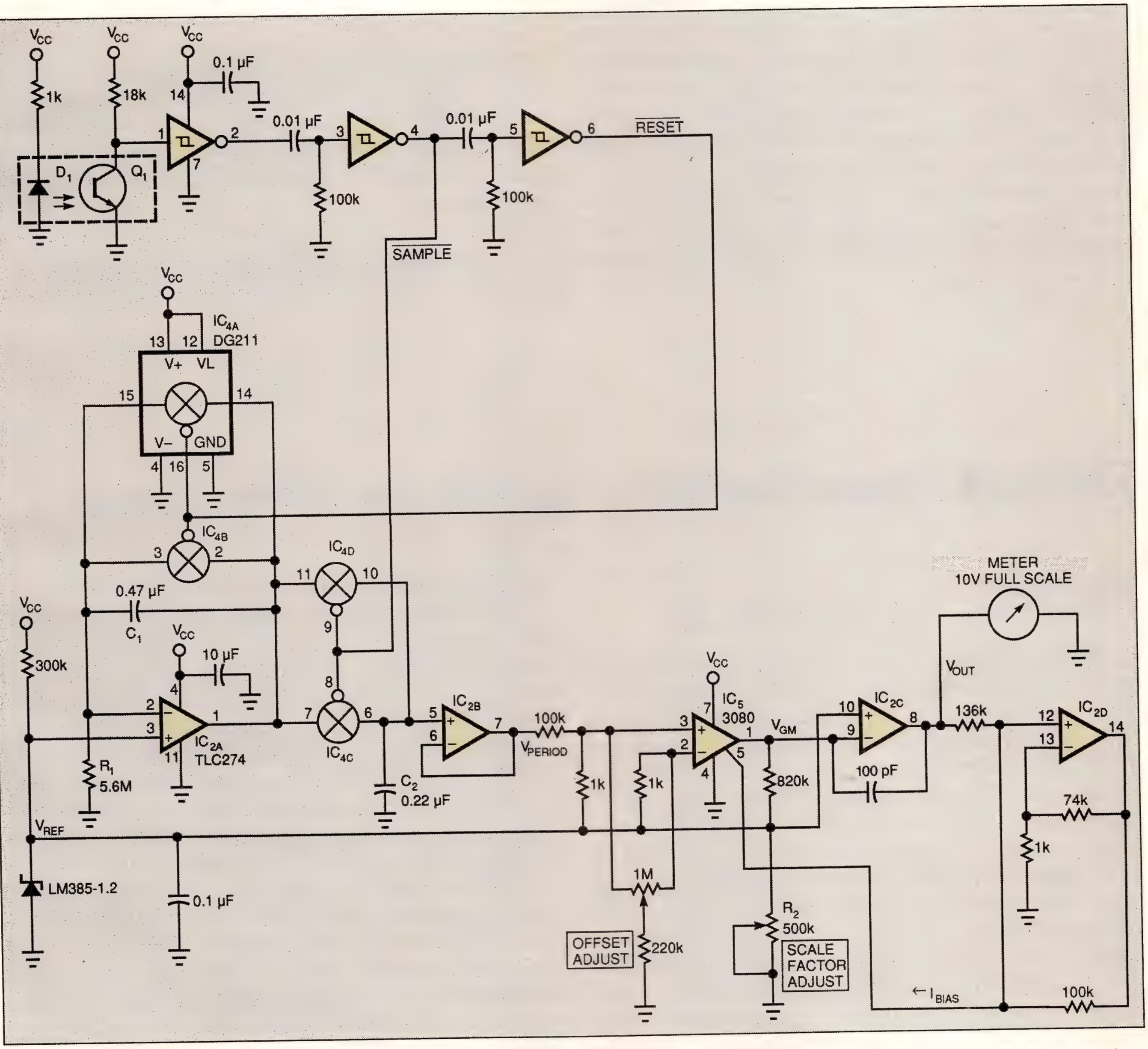


Fig 1—This ips meter relies on a transconductance multiplier, *IC_5, to generate a voltage inversely proportional to the period of rotation.*

1-msec-wide, sequential, nonoverlapping pulses—$\overline{\text{RESET}}$ and $\overline{\text{SAMPLE}}$—from the falling edge of each optointerrupter pulse. These two signals control the operation of the integrator comprising IC_{2A}, C_1, and R_1 through analog switches IC_{1A}, IC_{1B}, IC_{1C}, and IC_{1D}. The integrator in turn drives a S/H circuit consisting of another pair of switches, C_2, and a buffer amplifier.

If neither $\overline{\text{RESET}}$ nor $\overline{\text{SAMPLE}}$ is low, a current equal to V_{REF}/R_1 steadily charges C_1. When the optointerrupter generates a trigger pulse, $\overline{\text{SAMPLE}}$ goes low and switches IC_{4D} and IC_{4C} turn on momentarily, thus sampling the integrator's output voltage and storing it on C_2. Once $\overline{\text{SAMPLE}}$ goes high, $\overline{\text{RESET}}$ goes low, thus turning on IC_{4A} and IC_{4B}, which resets the integrator (IC_{4A} and IC_{4B} are connected in parallel to reduce their combined on-resistance). This sequence of events generates a dc voltage, V_{PERIOD}, proportional to the period of rotation at the output of the buffer amplifier, IC_{2B}. IC_5, a transconductance amplifier, acts as a 2-quadrant multiplier; it produces an output current proportional to the product of its input voltage and bias current. Since the output of this stage is a current, the voltage gain is a function of the load resistance. Thus, R_2 serves as a gain adjustment. IC_{2D} and its associated resistors form a modified Howland current pump and bias IC_5 at a level proportional to IC_{2C}'s output voltage.

The circuit forces the following relationships :

$$V_{GM} = V_{REF} \alpha V_{PERIOD} \times I_{BIAS}$$

and

$$I_{BIAS} \alpha V_{OUT}.$$

Thus,

$$V_{OUT} \times V_{PERIOD} \alpha V_{REF}.$$

Finally,

$$V_{OUT} = K/V_{PERIOD}, \text{ where K is a constant.}$$

To calibrate the circuit, run the machine at maximum speed and set the offset adjustment for an accurate output. Then, run the machine at its slowest speed and adjust the scale-factor potentiometer. Repeat this procedure until the reading is accurate at both speed extremes. EDN

To Vote For This Design, Circle No. 746

DRAM control scheme speeds memory access

Nagi Mekhiel
Definicon System Inc, Newbury Park, CA

By using both page and static-column mode and memory-bank interleaving, you can reduce the number of clock cycles necessary to retrieve DRAM (dynamic RAM) data. A standard DRAM page-mode access requires a precharge time delay before the controller can access a new row and column. Because this type of access is the slowest possible, call it SLOW. In static-column access, if the controller accesses a new column in the same row, it doesn't have to wait the precharge time. This access is the fastest possible; call it FAST. Interleaved-access schemes require the controller to access a new row and column for adjacent banks. However, the DRAM banks alternately precharge, so the controller doesn't have to wait the precharge time between each access. The time required for an interleaved access is somewhere between that required for SLOW and FAST, so call these accesses SLOW1.

Fig 1's timing diagram illustrates the various tradeoffs between these access schemes. Including any necessary wait states, a SLOW cycle typically takes 6 clock cycles (PCLKs), a FAST cycle 3 PCLKs, and a SLOW1 cycle 4 PCLKs. Designs that combine page and static-column access modes feature only FAST and SLOW accesses. Interleaved designs feature only SLOW and SLOW1 accesses. Thus, the average number of clock cycles for a page/static-column design, assuming FAST and SLOW accesses each occur 50% of the time, is $(3+6)/2=4.5$ cycles/access. The interleaved design requires $(4+6)/2=5$ cycles/access, again assuming SLOW1 and SLOW each occur 50% of the time. You could take advantage of both page/static-column and interleaved designs by implementing an access scheme in which FAST access occur 50% of the time, SLOW accesses 25% of the time, and SLOW1 access 25% of the time. Such a scheme would reduce the

average number of clock cycles to (3+(4+6)/2)/2 or 4 cycles/access.

Fig 2 shows a scheme for implementing such a combination of page, static-column and interleaving designs. The design uses multiple banks. Some are kept active for the page/static-column mode; others satisfy precharge-time interleaving. The block diagram divides the DRAM into two blocks, A and B, each of which have 4M bytes of memory selected by A_{22}. Each block consists of two banks selected by A_{12}. Each bank consists of a number of 4k-byte pages. The A and B row-address comparators detect an out-of-page access and generate the /HSA and /HSB signals. When the A and B control blocks sense that these high-speed access signals are active, the controller forgoes the precharge wait time. EDN

To Vote For This Design, Circle No. 747

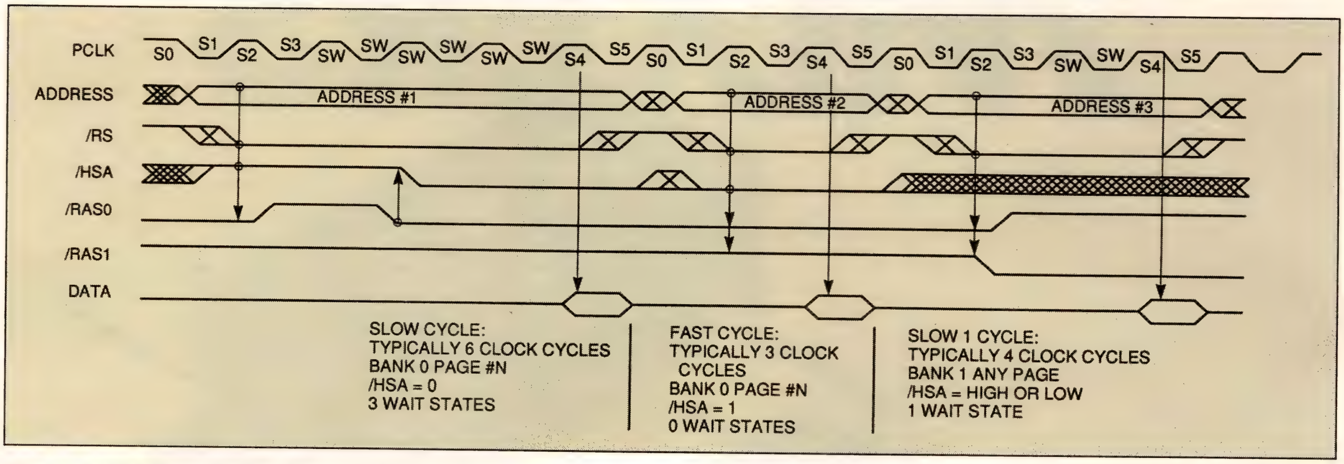


***Fig 1—A DRAM controller that combines** page access with the advantages of static-column access and interleaving (described here as SLOW, FAST, and SLOW1, respectively) can reduce the average number of cycles per access to 4.*

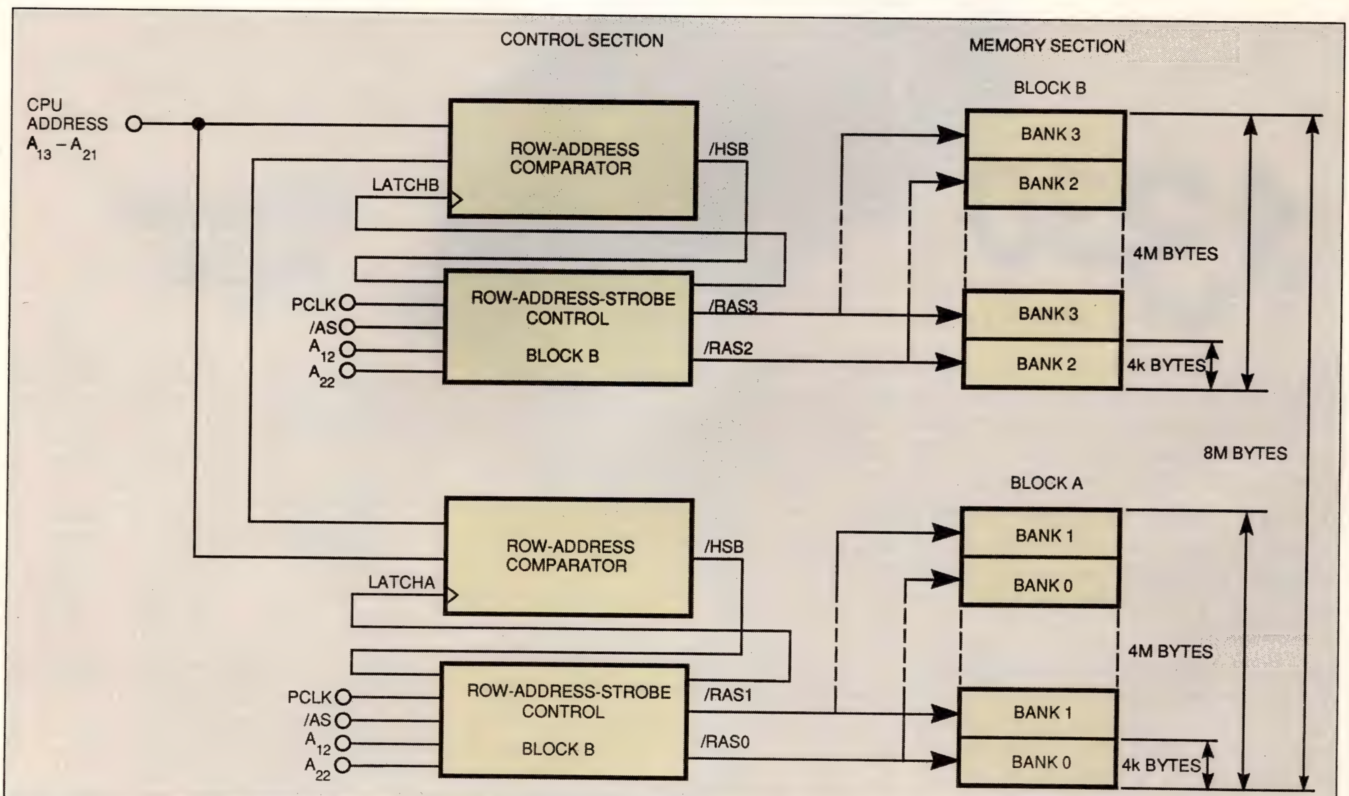
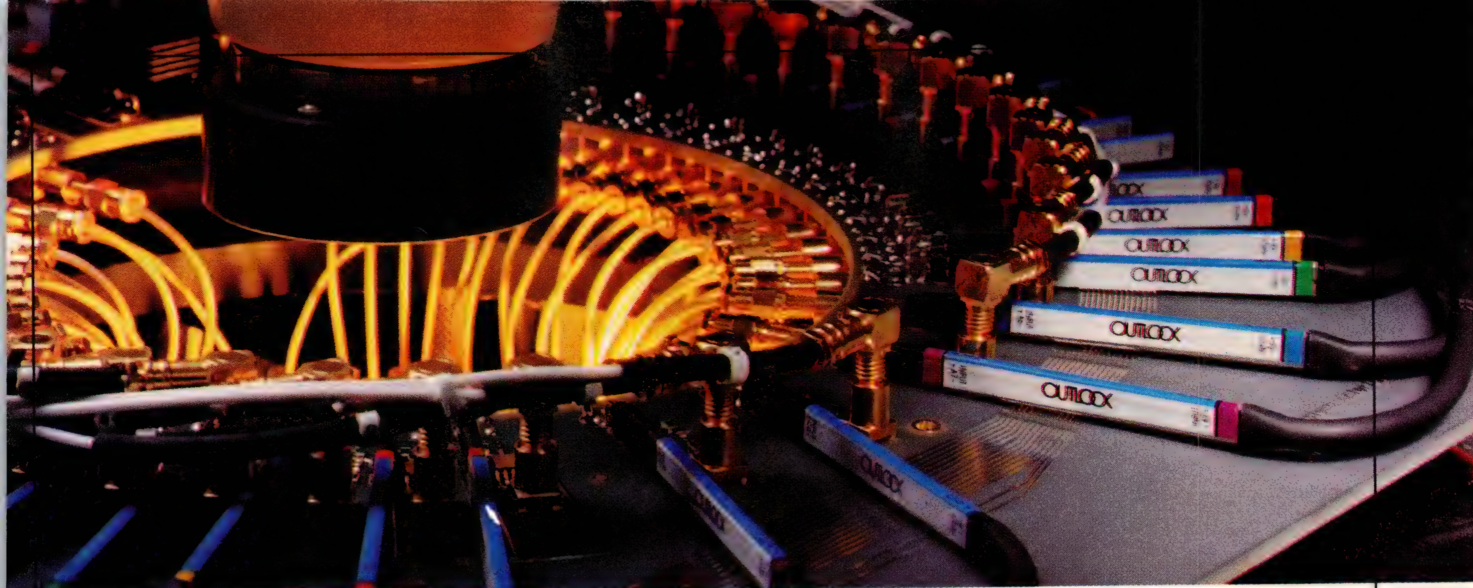


***Fig 2—This block diagram represents a design** that takes advantage of both page/static-column mode and interleaving by keeping some banks active for page/static-column mode while others undergo precharging.*



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NEW PRODUCTS

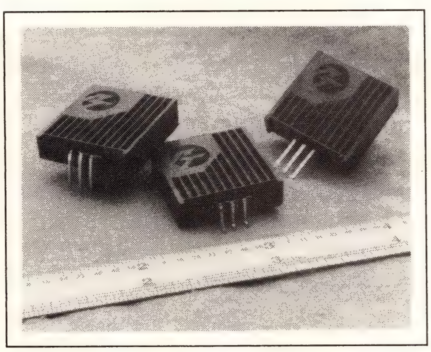
INTEGRATED CIRCUITS

4M-Bit Pseudo-Static RAM

- *Organized as 512k×8 bits*
- *Has advantages of DRAMs and SRAMs*

The HM658512 pseudo-static RAM (P-SRAM) combines the high density and low cost of a dynamic RAM (DRAM) with the interface simplicity and battery-backup capability of a static RAM (SRAM). Organized as 512k×8 bits, each memory cell of the 4M-bit P-SRAM has one transistor and one capacitor, which provides the low cost/bit generally associated with DRAMs. The device features a self-refresh mode that involves an on-chip timer and address counter, which transparently and automatically perform the refresh operation. Operating at 4V, this mode allows the use of a low-power, battery-backup function. In a 600-mil 32-pin DIP or a 525-mil 32-pin SO package, $90 (1000).

Hitachi America, IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (415) 244-7146. **Circle No. 351**



Switching Regulators To Replace 3-Terminal Types

- *Rated at 1.5A*
- *Have 90W/in.^{3} power density*

Called Integrated Switching Regulators, these devices provide a drop-in replacement for most linear regulators in TO-3 and TO-220 packages. A surface-mount package is also available. The current-mode devices, which operate at a frequency of 1 MHz, contain the control circuitry, an FET, a Schottky diode, and the inductor. Both positive and negative types are included in the line with voltage ratings of 5, 12, 15, and 24V. The company can also supply other voltages within this range as well as a special telecom version for −48V operation. Available initially in 1.5A ratings, the company will also be offering 3 and 5A versions later in the year. Featuring a power density of 90W/in.^{3} and an efficiency of >85%, the regulators come in 0.85×0.85×0.25-in. packages that normally require no extra heat sinking. $12 (1000).

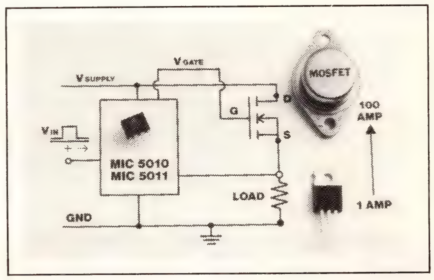
Power Trends Inc, 1020 Carolina Dr, West Chicago, IL 60185. Phone (708) 231-5505. FAX (708) 231-5577. **Circle No. 352**

High-Side Predrivers For N-Channel Power MOSFETs

- *Operate over a 7 to 36V power-supply range*
- *Include protection circuitry*

According to the company, its MIC5010/5011 predrivers offer a "one size fits all" approach to driving power MOSFETs in high-side-switching and power-control applications. Upon command of the logic input, the internal voltage tripler boosts the gate drive output as high as 20V above the system power supply. This action ensures that the gate of an external n-channel MOSFET switches solidly "on" to the system's high-side power supply. Both devices work over a power-supply range of 7 to 36V and feature overtemperature sensing and shutdown circuitry. Option pins allow the use of external capacitors to boost the switching speed and gate drive current. The MIC5010 also includes fault-detect and power-on reset functions as well as a programmable overcurrent sense comparator, which detects short circuits at the load and latches gate drive off until reset. MIC5010 in a 14-pin DIP, $2.25; MIC5011 in an 8-pin DIP, $1.95 (100).

Micrel Semiconductor, 560 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 245-2500. FAX (408) 245-4175. **Circle No. 353**



Disk Read-Channel Data Recovery Subsystem

- *25M-bps data-rate capability*
- *Maximizes read-data performance*

Combining signal conditioning and filtering with data qualification, the AD892 features a 25M-bps data-rate capability. The monolithic IC takes corrupted binary signals from the read-head preamplifier and produces recovered bits ready for synchronization. The IC contains a variable-gain amplifier (VGA), precision buffers, S/H circuitry, automatic gain control (AGC), trimmed comparators, and a 1-shot circuit to ensure a low bit-error rate. The VGA maintains a constant signal level with 30 dB of gain and a 40-dB control range. Read-head signal processing is handled by two 50-MHz buffer stages with gains of 12 dB; each buffer stage employs user-supplied filters. The hold circuit's fast acquisition allows AGC operation while the head is reading the disk sector header, thus maximizing performance. The amplified and conditioned signal is then compared to user-defined thresholds, and it clocks an output flip-flop if a valid

signal level occurs. The overall qualification scheme prevents single-bit error from propagating as a 2-bit error. In a 44-pin PLCC (plastic leaded chip carrier), $5 (10,000).

Analog Devices Inc, 181 Ballardvale St, Wilmington, MA 01887. Phone (508) 658-9400.

Circle No. 354

Dual 16-Bit DAC With Double-Buffered Latches

- *Interfaces to 8-bit μP buses*
- *Has 14-bit monotonicity*

Requiring no external parts to interface directly to 8-bit μP buses, the dual 16-bit DAC725 features 14-bit monotonicity and ±0.003% max integral-linearity error. Settling time for a full 20V step is 8 μsec max, and the device accepts data at rates as high as 10 MHz. The DAC725 incorporates dual double-buffered data latches, a precision buried-zener reference, D/A converters, and low-noise output op amps in a single 28-pin package. Input data is loaded in two 8-bit bytes. Separate lines for chip-select, latch-control, and clear functions provide design flexibility. Output range options are ±5 and ±10V. In a plastic DIP, $35.60; in a ceramic DIP, $75.62 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132. FAX (602) 889-1510.

Circle No. 355

8-Bit Flash A/D Converters

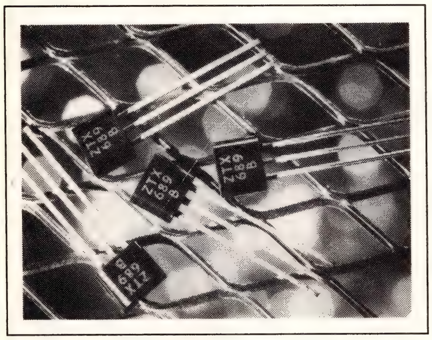
- *Input bandwidth is 150 MHz*
- *Have ±0.5 LSB linearity*

The ADC-32 and ADC-33 are monolithic 8-bit flash converters capable of digitizing analog signals with 100-MHz spectral components into digital words at a 150M-sample/sec conversion rate. Both units feature integral and differential linearity of ±0.5 LSB over the specified industrial or military temperature range. The ADC-33 includes additional reference taps, which offer better control of linearity over temperature. Output coding is user selectable for binary, complementary binary, 2's complement, and complementary 2's complement. Both devices operate from a −5.2V supply. The ADC-32 comes in a 42-pin ceramic sidebrazed DIP and is pin-compatible with the ADC-303 100-MHz 8-bit flash converter. The ADC-33 comes in a 48-pin ceramic sidebrazed DIP. In single quantities, from $143 for industrial-temperature versions; from $212 for military-temperature versions.

Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356.

Circle No. 356

COMPONENTS & POWER SUPPLIES



High-Gain Transistors

- *Have gain of 400 at 2A*
- *Feature low saturation voltage*

ZTX689B Super-E-line npn switching transistors feature gain figures of 500 and switching capabilities ranging to 2A at 120V. For example, the ZTX689B 20V unit has a gain of 400 with a collector current of 2A. At 100-mA collector current levels, minimum gain equals 500 for the entire line. Maximum saturation voltage levels range from 0.1V for the 45V ZTX690B to 0.25V for the 120V ZTX694B model. The units are housed in plastic TO-92 packages. £0.1 (100,000).

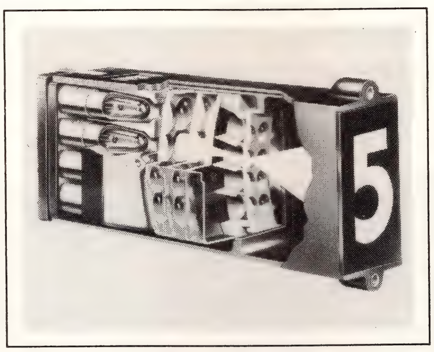
Zetex PLC, Fields New Rd, Chadderton, Oldham, OL9 8NP, UK. Phone 61 627 5105. FAX 61 627 5467. **Circle No. 383**

DC/DC Converters

- *Operate with 48V inputs*
- *Efficiency equals 78% min*

TC Series 10W dc/dc converters are designed for telecommunications applications. They operate from a 20 to 60V input (48V nom). Model 48S5.2000TC produces an output of 5V at 2000 mA; the output of Model 48S12.850TC is 12V at 850 mA: and Model 48S15.700TC has an output of 15V at 700 mA. Key specs include a 0.01% line regulation, 0.1% load regulation, 35-mV-typ output noise, 78% min efficiency, and 500V dc isolation. Automatic overtemperature protection is standard as is short-circuit protection. Featuring an operating range of −25 to +80°C, the converters are housed in 6-sided shielded cases to minimize radiation problems. $105.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (800) 542-3355; in CA, (415) 932-3911. FAX (415) 932-6017. **Circle No. 384**



Projection Displays

- *Display as many as 48 messages*
- *Are cascadable*

These projection displays can provide a variable-brilliance display for any image that's reproducible on film. The 15 models feature character heights ranging from 0.076 to 3.375 in. Display capacity ranges from 12 to 48 discrete messages; you can cascade individual models into multimodule assemblies for added information display capacity. The modules can accommodate lamps ranging from T-⅞ to T-3¼ in size. Most of the display models can withstand temperature and shock in accordance with MIL-STD-202 and vibration as described in MIL-STD-167-1. Self-contained driver/decoders are available as an option as well as military-grade configurations. $36 to $168 (100). Delivery, eight to 10 weeks ARO.

IEE Inc, Planar Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. FAX (818) 902-3723. **Circle No. 385**

Intelligent Displays

- *Feature a 2-in.-high character*
- *Are TTL compatible*

The ISDS20135 Series units are 2-in.-high, single-character 5×7 dot-matrix intelligent displays. The built-in CMOS IC contains memory, ASCII character generator, and LED multiplexing and drive circuitry. These displays have a 96-ASCII-character repertoire and are TTL and μP compatible. You can cascade the units to develop multicharacter displays. ISDS20135 displays are available in three colors. High-efficiency red units, $17.14; green units, $19.77; ultrabright red units, $22.34 (100).

Isocom Inc, 256-H E Hamilton Ave, Campbell, CA 95008. Phone (408) 370-2212. FAX (408) 370-2309. **Circle No. 386**

High-Side Predrivers

- *Work with any FET*
- *Have internal thermal-protection circuitry*

The MIC5010 and MIC5011 predrivers will drive any FET in a high-side switching and power-control application. The devices each have an internal voltage pump that supplies high-side voltage drive as much as 20V higher than V_{DD}. The drivers operate with supplies of 7 to 36V and feature pins that allow you to use external capacitors to boost the switching-speed and gate-drive current. Both units include temperature sense and shutdown circuitry. The 5010 features a pro-

grammable overcurrent sense comparator that detects short-circuit conditions at the load and latches gate drive off until reset. The 5010 also has a fault-detect output and power-on reset. Operating range spans −40 to +85°C. MIC5010BN, $2.25; MIC5011BN, $1.25 (100).

Micrel Semiconductor, 560 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 245-2500. FAX (408) 245-4175. **Circle No. 387**

Full-Travel Keyboard

- *Compatible with IBM PC, PC/XT, PC/AT, and PS/2*
- *Comes in rack-mount package*

The R-19 full-travel keyboard is compatible with IBM PC, PC/XT, PC/AT, and PS/2 computers. Designed specifically for use in hostile environments, the unit has an IP (international protection) rating of 54 and is impervious to dust and liquid spills. The IP rating is achieved through the use of molded silicone-dome technology combined with sealed electronics and state-of-the-art membrane technology. Additional features include 12 function keys, a 19-in. rack-mount package, separate cursor keys, frequency-programmable autorepeat for all keys, N-key rollover, and positive tactile feel. $345.

Preh Electronic Industries Inc, 470 E Main St, Lake Zurich, IL 60047. Phone (312) 438-4000. FAX (312) 438-5522. TLX 297112.
Circle No. 388

Fiber-Optic Receiver

- *Has a 1.5-mile transmission capability*
- *Features a choice of connector styles*

This 50M-baud fiber-optic receiver completes the company's 5- to 50M-baud fiber-optic link family. Featuring a minimum optical sensitivity of −35 dBm, the TTL-compatible receiver will operate over distances of 1.5 miles min. Over shorter distances, the unit will handle higher data rates. All receivers include a link-status indicator that indicates when the optical signal drops below the minimum operating sensitivity level. The unit operates in the 860-

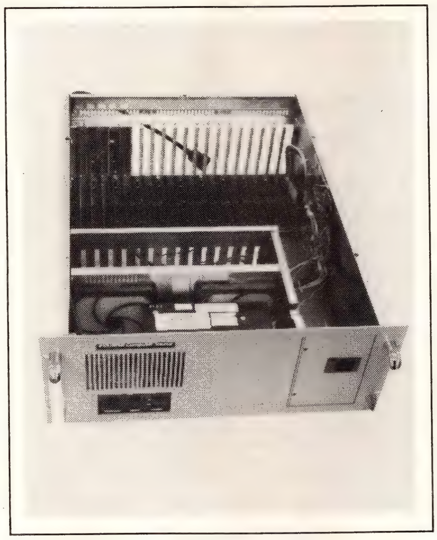
nm range and is housed in a 14-pin plastic DIP. $69 (50,000).

Siemens Fiber Optic Components, 3846A First Ave, Evansville, IN 47724. Phone (812) 422-2322. **Circle No. 389**

Industrial-Grade Chassis

- *Includes a backplane*
- *Holds two drives*

The 7520-32V rack-mountable chassis incorporates an IBM PC-compatible backplane, which features 20 PC/AT slots. The unit houses two half-height, floppy- or hard-disk drives in a vertical position. The chassis also includes a 315W power supply, which features automatic 110/220V selection. Also included are a fused ac receptacle and a front-panel keyboard connector. Two temperature-controlled 120-cfm fans pressurize the chassis to exclude dust and dirt. The 6-layer construction provides termination resistors on all lines, and the metal door protects the drives. A tabletop version is also available. $1795.



Industrial Computer Source, 4837 Mercury St, San Diego, CA 92111. Phone (619) 279-0084. FAX (619) 541-1138. **Circle No. 390**

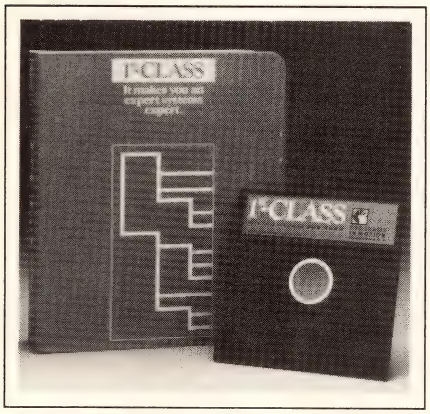
Panel Display

- *Includes drive electronics and a controller*
- *Displays 336 characters*

The APD-336M019 dot-matrix display-panel module includes drive electronics and a controller. The controller provides refresh memory, character generation, and control logic to enable the module to serve as a direct readout. The unit displays 336 5×7 dot-matrix characters arranged in 14 rows×24 columns. The display has a 70-fL brightness and a 120° viewing angle. Other features include a parallel ASCII interface and character-blink mode. The display is available in commercial or extended temperature versions. Input voltages are 5 and 15V. $740 (100). Delivery, 12 to 14 weeks ARO.

Dale Electronics Inc, Box 609, Columbus, NE 68602. Phone (402) 563-6275. **Circle No. 391**

CAE & SOFTWARE DEVELOPMENT TOOLS



Expert System Development Tools For OS/2

- *Serve both novices and experts*
- *Provide hypertext retrieval for associative access by users*

Fusion is a set of tools for developing expert systems. It uses a spread-sheet technique that lets you build a table of the factors affecting the value of a result. From the table, you can build rules, or decision trees, and chain them together to build a knowledge base. Then, the Advisor program runs a consultation in which it asks the questions you have defined, reasons forward or backward, and presents the advice you've defined. A hot-key feature allows you to switch rapidly back and forth between the Advisor and the process of building and modifying the decision trees. The HT development tool offers all of the features of Fusion plus a hypertext feature that lets developers control large quantities of textual information in a manner permitting end users easy associative access to it. HT is intended for applications that require extensive, context-sensitive help functions. Both Fusion and HT are available for all OS/2- and MS-DOS-based personal computers. Fusion, $1495; HT, $2495.

1st-Class Expert Systems Inc, 526 Boston Post Rd, 150-East, Wayland, MA 01778. Phone (508) 358-7722. FAX (508) 358-4395.

Circle No. 392

Real-Time Unix For The Mac

- *Supports TCP/IP Network software and the X Window System*
- *Runs on all Macintosh computers*

UniFlex is a real-time, Unix-compatible operating system for computers based on the Motorola 680x0 family of μPs. It provides multiuser and multitasking capabilities and comes with a full set of software-development tools, a C compiler, TCP/IP (transmission control protocol/internet protocol) network-support software, and the X Window System version 11.3. The TCP/IP networking software works with the Apple Ethertalk board and includes a large selection of popular networking utility programs such as FTP, Rsh, Rlogin, Telnet, Mail, and Sendmail. The package also includes a C library of Berkeley-style socket functions for the use of developers writing network-based application software. Single-system development license, $595.

Technical Systems Consultants Inc, 111 Providence Rd, Chapel Hill, NC 27514. Phone (919) 493-1451. FAX (919) 490-2903.

Circle No. 393

DSP Simulator/Debugger

- *Simulates the TMS320C25 architecture in software*
- *Runs on IBM PCs and compatibles*

zSIM320C25 is a simulator/debugger for TI's TMS320C25 digital signal processor. The program runs on IBM PCs and compatibles and simulates the internal architecture of the DSP chip. It can execute DSP programs in either Intel Hex or TI Tag format. You have access to the full 64k bytes of program and data memory, and you can modify all registers, flags, and I/O ports, as well as program, stack, and data memory. You can redirect I/O data to disk files; a trace buffer lets you examine the last 200 instructions executed. Execution commands let you step through or around subroutines, and you can set breakpoints to stop execution when specified conditions are met. You can also execute DOS commands without leaving the simulator program. On-line help screens provide easy reference to all simulation commands. $395.

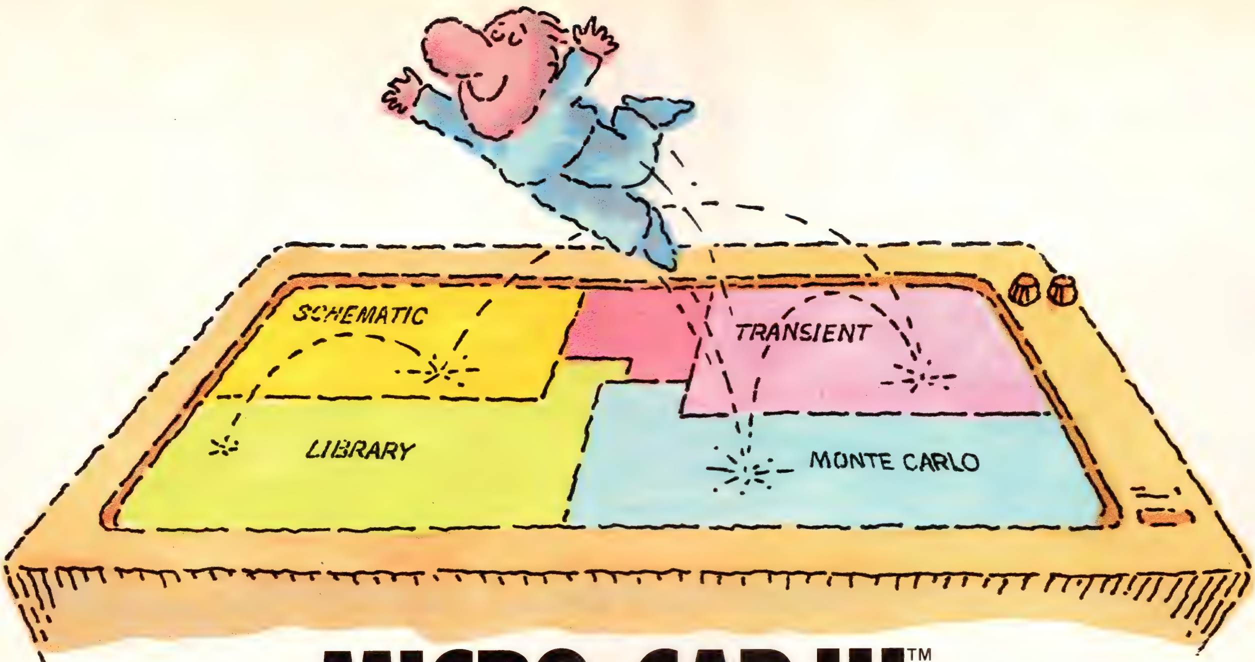
ZTech Systems, 2520 Voorhies Ave, Brooklyn, NY 11235. Phone (718) 403-4755. **Circle No. 394**

VHDL Development System

- *Runs on VAX/VMS and Sun 3 systems*
- *Provides a Make facility that allows automatic recompilation*

The VHDL Support Environment version 2.1 consists of a VHDL analyzer, a design-library manager, a VHDL library system, and a VHDL simulator. It allows you to design, simulate, and document systems, boards, and chips, using all of the features of the VHSIC Hardware Description Language. The new version, which runs on VAX/VMS and Sun 3 computers, provides a 40% speed increase in the VHDL simulator. A Make facility allows automatic recompilation of design units and generates all design units in a model without requiring you to specify the order of model-generation. Other enhancements include the ability to break on delta cycles and to view composite signals. Some new commands also simplify the setting of default path names. From $12,000.

Intermetrics, 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-1840. **Circle No. 395**

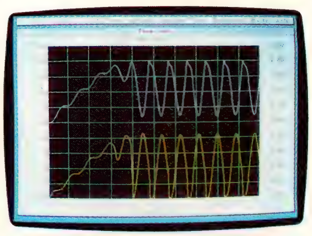


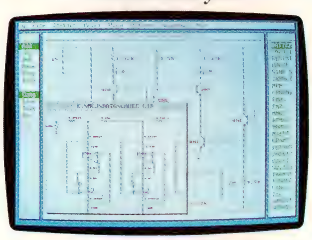
MICRO-CAP III.™ THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

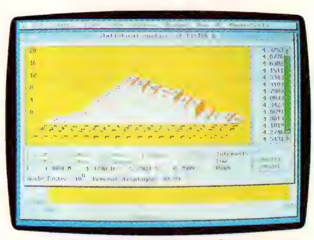
MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

The program's window-based operation and schematic editor make circuit creation a breeze. And super-fast SPICE-like routines mean quick AC, DC, Fourier and transient analysis — right from schematics. You can combine simulations of digital and analog circuits via integrated switch models and macros. And, using stepped component values, rapidly generate multiple plots to fine-tune your circuits.

We've added routines for noise, impedance and conductance — even Monte Carlo routines for statistical analysis of production yield. Plus algebraic formula parsers for plotting almost any desired function.


Transient analysis


Schematic editor


Monte Carlo analysis

Modeling power leaps upward as well, to Gummel-Poon BJT and Level 3 MOS — supported, of course, by a built-in Parameter Estimation Program and extended standard parts library.

There's support for Hercules,® CGA, MCGA, EGA and VGA displays. Output for laser plotters and printers. And a lot more.

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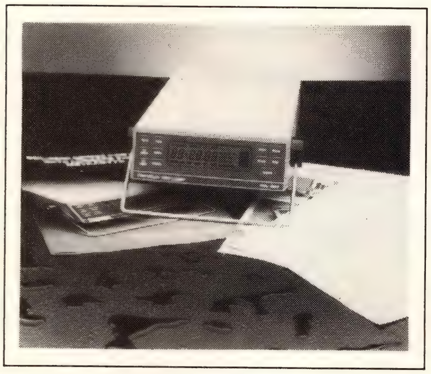
CIRCLE NO. 82

TEST & MEASUREMENT INSTRUMENTS



Data Loggers

- *Connect to sensors or signal conditioners*
- *Continuously monitor alarm limits at 4-sec intervals*

When delivered, data loggers in the DDL-4000 series are ready to collect data without programming. The loggers connect directly to sensors, such as thermocouples, as well as to the outputs of signal conditioners. In addition to 16 analog inputs with switch-selectable gain, cold-junction compensation, and linearization, each unit has four digital inputs that can sense logic levels or contact closures. Each unit also has 16 logic-level alarm outputs. Even if you ask the logger to transmit data only once a day, it will constantly monitor its analog inputs and compare them every 4 sec to alarm limits stored in nonvolatile memory. All units have an RS-232C port; a master can control four expansion loggers, which can have blank front panels. From $1440.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 357**

VXIbus PC With Ethernet Interface

- *Includes 80386, 40M-byte hard disk, and IBM VGA graphics*
- *Software allows multiple VXI systems to communicate*

The EPC-2e is an 80836-based computer in a double-width VXIbus module. Units are available whose CPUs operate at 16 and 20 MHz. The module includes an Ethernet interface that lets you link VXIbus-based instrument systems with each other and with other network-based systems such as CAE workstation networks. The computer also incorporates a floppy-disk drive, a 40M-byte hard disk, a graphics adapter compatible with the IBM VGA, parallel and serial ports, and room for 8M bytes of RAM. The vendor has also announced an MS-DOS-based software package called VXI Network Bridge, which loads automatically when you apply power to the computer and also enables multiple VXI mainframes to communicate. Computer, from $8550; software, $1000/network.

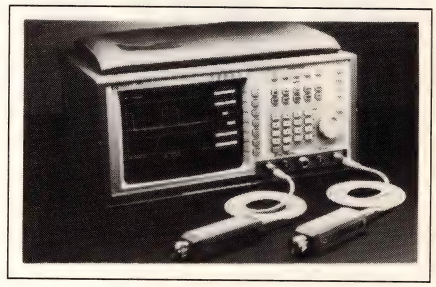
Radix Microsystems Inc, 19545 NW Von Neumann Dr, Beaverton, OR 97006. Phone (503) 690-1229. FAX (503) 690-1228. **Circle No. 358**

Instrument Plug-In Cards For IBM PCs And PS/2s

- *Include data-acquisition and special-function cards*
- *Work with signal-conditioning panels*

The PC-Test card series includes members for the IBM PC bus and for the IBM PS/2 series' MCA (Micro Channel Architecture) bus. Among the types are a high-speed scope, a multifunction data-acquisition card, two 32-channel digital I/O and counter cards, a relay actuator card, a 6-channel analog output card, a stepper-motor control card, an RS-422/RS-485 interface, two IEEE-488 interfaces, an arbitrary-waveform generator, a voice-output card, and a RAM/ROM disk card for use in dirty environments where electromechanical disk storage units would behave unreliably. External signal-conditioning panels provide such functions as screw-terminal inputs and optical isolation. From $150.

Soltec Corp, 12977 Arroyo St, San Fernando, CA 91340. Phone (800) 423-2344; in CA, (818) 365-0800. **Circle No. 359**



RF/Microwave Peak-Power Analyzer

- *Operates at frequencies as high as 40 GHz*
- *Measures 13 pulse parameters*

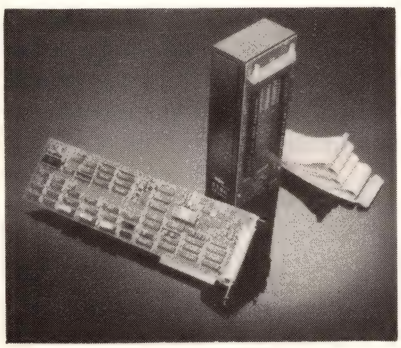
The HP 8990A peak-power analyzer works with pulsed RF carriers at frequencies as high as 40 GHz. The instrument performs many more functions than do peak-power meters. It can, for example, measure 13 pulse parameters at rates of 35 to 65 measurements/sec. The unit has a 4-channel scope display, including two channels that display detected RF waveforms. The other two channels have 100-MHz bandwidth and allow you to view trigger pulses and video waveforms. By basing its signal processing on data acquired at 10M samples/sec, the analyzer can characterize single-

INSTRUMENTS

shot pulses. Root-sum-squared instrumentation uncertainty is ±4%; sensor-calibration uncertainty is ±2% at 4 GHz and ±5% at 40 GHz. The power sensors have a VSWR of 1.35 at 26.5 GHz. $15,000; sensors, $1400 to $1900. Delivery, eight weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 360



Data-Acquisition Board For IBM PCs

- *Provides 16 analog-input channels and three counter/timers*
- *Optionally includes two D/A converters*

The 5525MF is a low-cost data-acquisition board for the IBM PC bus. It accommodates 16 analog inputs, permits user selection of signal gain, and makes 25,000 12-bit A/D conversions/sec. DMA-controlled data transfers are supported. The board also includes three pulse/frequency counters and, optionally, can include a pair of D/A converters. The vendor supplies accessories such as signal-conditioning panels, and ships the application software package Labtech Acquire with each board. $495.

Adac Corp, 70 Tower Office Park, Woburn, MA 01801. Phone (800) 648-6589; in MA, (617) 935-6668. FAX (617) 938-6553.

Circle No. 361

EL LAMP INVERTERS

GET MORE FROM ELS

- *Reverse polarity protected*
- *No-load protected*

A self-adjusting DC-AC inverter that matches performance to EL lamp capacitance changes, to extend lamp-life and optimize brightness. (For more information, see Loctite ad, below.)

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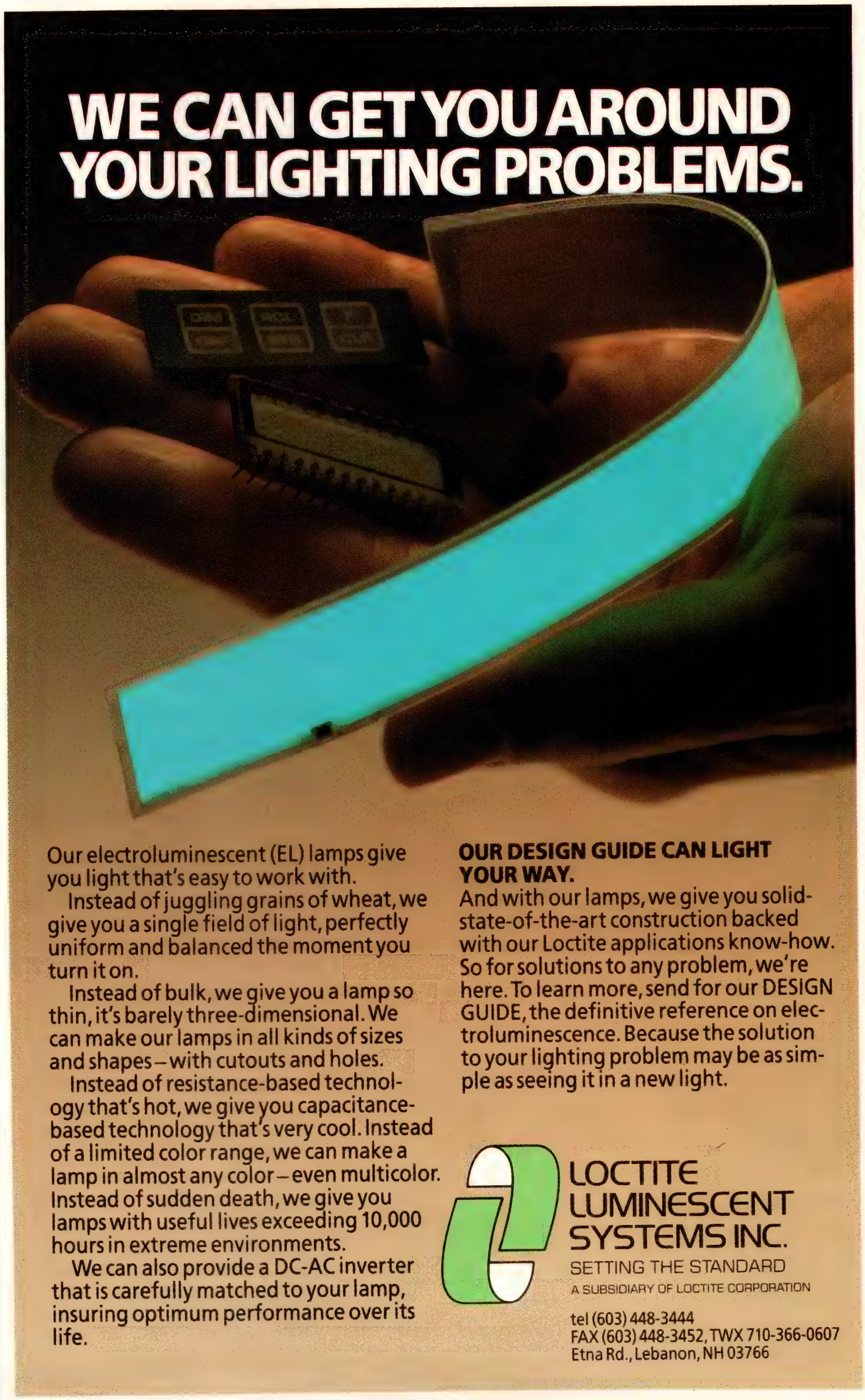


CIRCLE NO. 83

STD Bus CPU Board

- *Has a 16-MHz 80C186 μP and 2M bytes of DRAM*
- *Software development package generates C language code*

The Model 8700 CPU board for the STD Bus features a 16-MHz 80C186 μP and 2M bytes of dynamic RAM. Two ROM sockets accept 27512 or 27C010 EPROMs. The board conforms to the 16-bit STD Bus specification and is compatible with 8-bit STD boards. It comes with a debug program, which allows for firmware development on an IBM PC-compatible computer. You can link the CPU board to the PC through a serial communications card with an RS-232C port, such as the company's model 7060-3. An optional hardware and software package, called C-Engine, lets you develop C language code using Borland's Turbo C Professional package. Interface software lets you load the code into EPROM. In addition, the board has a watchdog timer that restarts a program in an orderly manner if a power glitch occurs. $995.

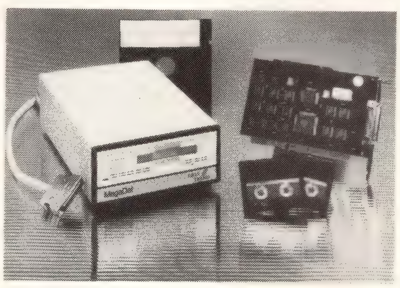
Cubit, 340 Pioneer Way, Mountain View, CA 94041. Phone (415) 962-8237. FAX (415) 965-9355. TLX 797377. **Circle No. 362**

Video Frame Grabber

- *Transfers data to and from a host via SCSI*
- *Captures video signals in NTSC, PAL, and RS170*

The DASM-FGM stand-alone video frame grabber communicates with a host via SCSI by emulating a RAM disk. Because it uses SCSI, the unit can function with a variety of hosts, such as those manufactured by Sun Microsystems, DEC, Hewlett-Packard, Apple, and IBM. The unit consists of a controller card packaged in a form factor that fits into a half-height drive bay. The controller card contains a 68008 μP, as much as 8M bytes of video memory, and SCSI and DMA controllers. The frame grabber digitizes video input signals conforming with NTSC, PAL, and RS-170 formats. It can store data in real time at 30 frames/sec. A partial-screen capture mode permits the capture of a rectangular sub-area of the video input image. A multiple-resolution capture mode, captures 512×512-, 256×256-, or 128×128-pixel images. With 256k bytes of RAM, $2995; with 8M bytes of RAM, $6500.

Analogic CDA Div, 8 Centennial Dr, Centennial Industrial Park, Peabody, MA 01961. Phone (508) 977-3030. FAX (508) 977-9220. TLX 6817408. **Circle No. 363**



DAT Storage System

- *Uses a 4-mm cassette to store 700M bytes*
- *Can randomly access files in less than 60 sec*

The MegaDat digital-audio-tape (DAT) storage system uses a 4-mm, credit-card-sized cassette to store 700M bytes of data. The cassette stores the equivalent of more than 10 60M-byte ¼-in. cartridges. The system interfaces with a 16-bit ISA (industry standard architecture) bus and operates with a workstation that has DOS 3.X, 1M byte of RAM, a local hard-disk drive, an unused 16-bit expansion slot, and a power connector. The DAT also works with Novell Netware 2.0 or higher software, which is menu driven with context-sensitive help commands. Other features include a random file-access time of <60 sec and error checking with correction. Internal version, $2750; external table-top version, $2950.

GigaTrend, 2234 Rutherford Rd, Carlsbad, CA 92008. Phone (619) 931-9122. FAX (619) 931-9959. **Circle No. 364**

Industrial IBM PC

- *Has 20 expansion slots in a 19-in. rack-mount chassis*
- *Two half-height drives can be mounted behind a protective door*

The Model 7520-32V is an industrial IBM PC-compatible computer. It consists of a 19-in. rack-mount chassis, made of heavy-gauge steel and containing 20 AT-style expansion slots. You can mount two half-height storage drives behind a protective door in the chassis. The chassis comes with a 315W power supply, which operates from 47- to 440-Hz line frequencies, and with selectable 110 and 220V ac. Two 120 cfm fans cool the main chassis and the power supply. Both fans have filters and are temperature controlled. The fans build up a positive pressure inside the chassis, which prevents dust particles from entering through crevices. The chassis measures 19×24×7 in. $1795; table-top version, $1795.

Industrial Computer Source, 4837 Mercury St, San Diego, CA 92111. Phone (619) 279-0084. FAX (619) 541-1138. **Circle No. 365**

68030-Based Computer

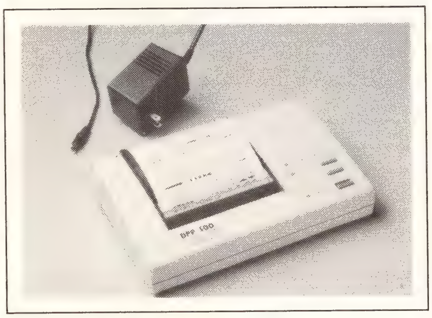
- *Runs at 25 MHz and serves eight to 32 active users*
- *Operates with release 3.2 of TI's System V operating system*

The 1505 is the latest member of the company's 1500 series of multiuser computers. The computer can serve from eight to 32 active users. The floor-standing base unit comes with a 25-MHz 68030 μP, a 25-MHz

68882 floating-point unit, a 64k-byte cache-memory, a 150M-byte cartridge-tape backup system, and 4M bytes of RAM that can be expanded to 16M bytes. You can order the base system with a 5¼-in. hard-disk drive that has either a 182M-, 380M-, or 760M-byte capacity and a SCSI-2 port. As many as three additional mass-storage devices can be connected to the computer, each containing a maximum of five 380M- or 760M-byte disk drives and a tape backup unit. Maximum available storage is 4.56G bytes. The computer runs with release 3.2 of the company's System V operating system, which provides support for a TCP/IP (transmission control protocol/internet protocol) link and Network File System software. $12,900 with a 182M-byte hard-disk drive.

Texas Instruments Inc, Information Technology Group, Box 202230, ITG-030, Austin, TX 78720. Phone (800) 527-3500.

Circle No. 366



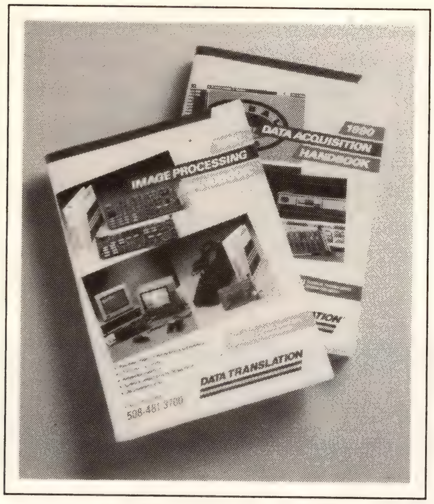
Dot-Matrix 40-Column Printer

- *Prints a 256-character set*
- *8k-byte buffer memory switches to either a serial or parallel port*

The DPP-500 thermal dot-matrix printer communicates with computers, dataloggers, and programmable logic controllers through either an RS-232C port or a Centronics parallel port. You can switch either port to an internal 8k-byte buffer memory. The user can configure the serial port to communicate at baud rates as high as 9600. The benchtop 40-column printer prints a 256 ASCII character and graphics set; you can address individual dots for custom graphics. The printer operates from either a 110V ac outlet by using a supplied wall adapter or from an internal battery pack that recharges when the wall adapter is plugged in. The DPP-500 prints at 37.5 cps in standard mode and 50 cps in condensed mode. Its standard graphics mode has a resolution of 320 dots/line, while its condensed graphics resolution is 640 dots/line. $442; paper, $4.25.

Acculex, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3660. TLX 503989.

Circle No. 367



Data-Acquisition And Image-Processing Handbooks

The 480-pg *1990 Data Acquisition Handbook* provides information about the vendor's data-acquisition and array-processing products, including analog and digital I/O products for IBM PCs, PC/XTs, PC/ATs, and compatible computers; the IBM PS/2; Macintosh II; Sun; MicroVAX; Multibus; and STD Bus computers. The 352-pg *1990 Image-Processing Handbook* focuses on image-processing products, including frame-grabber boards, frame processors, and image-processing software for IBM PCs and compatibles, MicroVAX, Sun, and VME-bus computers. Both catalogs present detailed data sheets, product summary tables, and application notes and describe more than 600 boards, software packages, and accessories.

Data Translation, 100 Locke Dr, Marlboro, MA 01752.

Circle No. 377

Catalog For PC Users

The vendor's catalog (90-1) features electronic-design programs, including logic simulation, pc-board design, filter design, and network analysis. Other offerings include AutoCAD engineering symbols and utilities, an HVAC (heating, ventilating, air conditioning) design system, and three CAD systems. Some of the engineering programs listed are preventive maintenance, statistical process control, surveying, logarithmic graphing, and statistical analysis.

Sector Systems Co Inc, 416 Ocean Ave, Marblehead, MA 01945.

Circle No. 378

Offering Of Power-Supply Products

The company's 1990 catalog highlights its expanded line of single- and multiple-output switching power supplies and dc/dc converters ranging from 160 to 175W. Standard lines have acquired several new models, and other product lines feature an ac automatic line-selection option. The publication provides specifications, ratings, outputs, and schematics.

Todd Products Corp, 50 Emjay Blvd, Brentwood, NY 11717.

Circle No. 379

Digital-Logic-Analyzer Products Categorized

The vendor's full-line catalog describes its logic analyzers based on PCs. The publication explains that the analyzers are available as complete instruments with integrated IBM PC/XTs, PC/ATs, and 80386 personal computers; as portable analyzers connected to laptop PCs; or as peripherals to add to current PCs. The document highlights six models for any application; optional 16-channel, 20-MHz pattern generation; and data-compare functions.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103.

Circle No. 380

Extensive Listing Features T&M Products

The company's 1990 catalog presents 20 new products, a rack-mount selection guide, a glossary of terms, and a section on abbreviations and symbols. Besides descriptions of the products, the 536-pg publication contains photos and ordering information for more than 650 products, accessories, and software programs. Combining product lines with those of its European counterpart, the company's catalog offers 18 major product categories, as well as technical literature and a listing of worldwide sales offices. The index provides both alphabetical and numerical listings of all products and services.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206.

Circle No. 381

Selecting A Flat-Panel Display And A CRT Monitor

The latest book in the Designer's Guide Series, *How to Select a CRT Monitor*, follows publication of its predecessor, *How to Select a Flat Panel Display*. Combined, the two volumes provide more than 700 display models in print and on disk. Both books contain concise, illustrated technical-reference material on CRT and flat-panel-display technology. Both forms of the publications receive periodic updates.

Beta Review Inc, Box 38, Millwood, VA 22646. **Circle No. 382**

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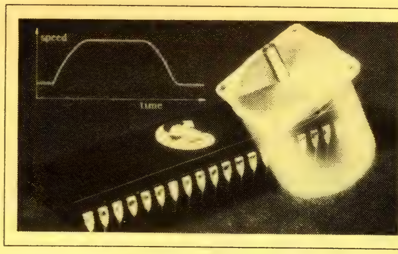

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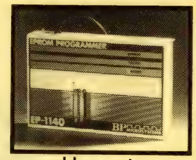

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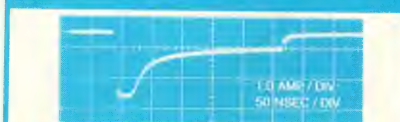

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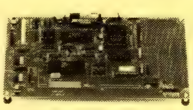

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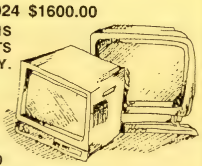

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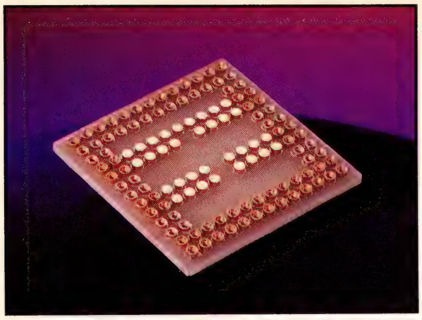

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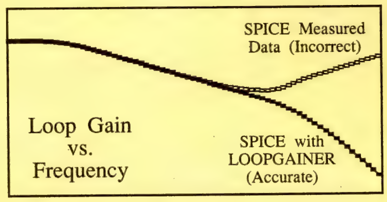

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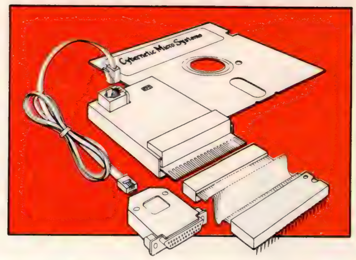

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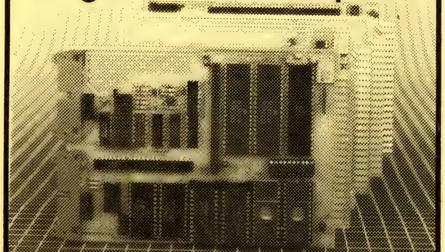

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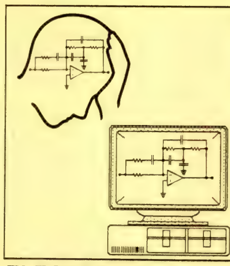

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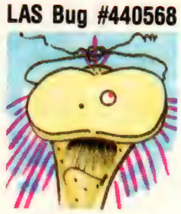

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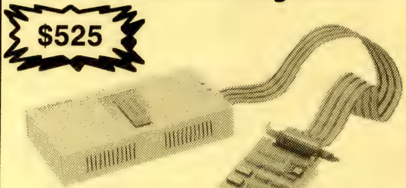

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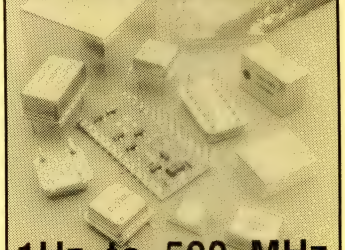

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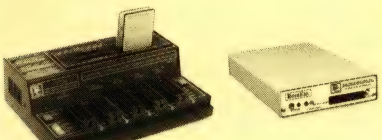

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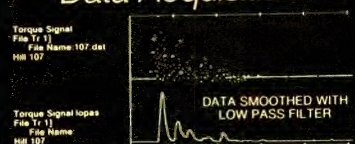

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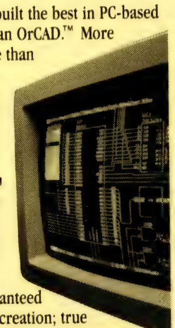

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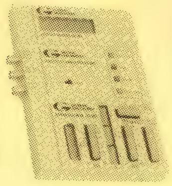

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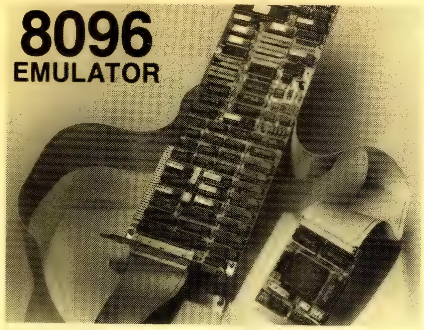

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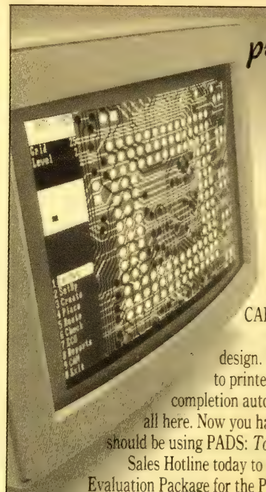

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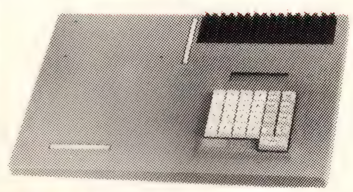

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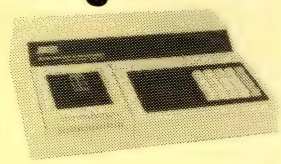

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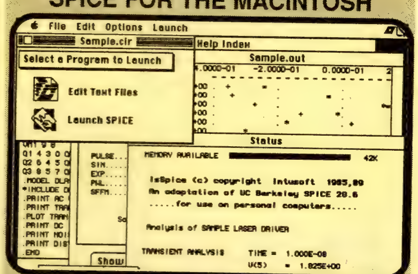

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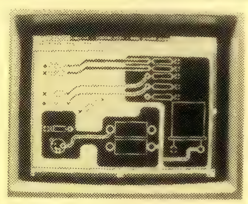

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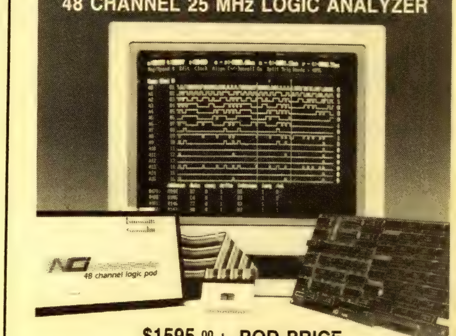

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An engineer's guide to marketing

Jay Fraser, *Associate Editor*

Gone are the days when an engineer could develop a device in isolation, turn it over to someone in manufacturing, and forget about it. Today's engineer has to understand not only how a new product is conceived, manufactured, and tested, but also how it is marketed, sold, and serviced. This more extensive knowledge can be a crucial factor in the success of a company's products and the success of an engineer's career.

Marketing is one of those business activities that drives some engineers to distraction. The concept of marketing tends to be ill-defined and fuzzy. Almost anything that contributes to selling a product or a service—from package design to public relations—can be called part of marketing.

"It is ill-defined and fuzzy in some ways. That's one of the nice things about it," says William Schweber, senior technical marketing engineer at Analog Devices in Norwood, MA. "A lot of marketing is based on intuition and experience, educated guesses, and not-so-educated guesses."

Like many marketers in high-tech firms, Schweber is an engineer. He holds a BSEE from Columbia University (New York, NY) and an MSEE from the University of Massachusetts (Amherst). He worked in hardware design and hardware/software integration of real-time systems at companies such as GTE/Sylvania and Instron. "At Analog Devices virtually everybody in marketing has been a working engineer," he says. "You have to have not only a technical background, but you have to have spent a couple of years in the trenches as a designer."

Another aspect of marketing that bothers some engineers is that it doesn't deal with hard facts and figures or easily measurable results. It's difficult to determine how much of sales is due to the marketing effort and how much to the quality of the product.

"Marketing is not an exact science," says Mike Collins, marketing manager of the Microprocessor Products Group of Motorola Inc (Austin, TX). "It's not like engineering, where you can design a circuit and model it and test it and strive for perfection. In marketing, some questions don't have answers, and you're not always working with perfect information."

Although it's probably impossible to come up with a brief definition that will satisfy everyone, market-

The first in an occasional series exploring aspects of modern business.

ing can be described as all those business activities that are designed to direct the flow of goods and services from producer to consumer.

"It's all too easy from an engineer's perspective to think that marketing consists solely of producing a clearly written data sheet, getting it printed, and mailing it to anyone who asks for it," says Schweber. "That's only one small aspect of marketing. There's much more. Not only what can we do or what do we want to do, but what do people want and why do they want it? And how do we differentiate ourselves from others offering similar products?"

Marketing is as old as civilization. As soon as people began to barter goods, they became involved in a simple form of marketing. Until the 20th century, business, in general, had a production orientation. The relative scarcity of goods meant there was seldom a shortage of buyers. Demand almost always exceeded supply.

In those days companies concentrated on improving their products, because superior products would automatically attract customers. Marketing and sales efforts were minimal, because it was widely believed that a good product would sell itself. That attitude was summed up in Ralph Waldo Emerson's famous saying: "If a man writes a better book, preaches a better sermon, or makes a better mousetrap than his neighbor, though he builds his house in the woods, the world will make a beaten path to his door."

What's true in one century isn't necessarily true in the next, and marketing changed greatly after World War I. The invention of the assembly line and other modern production techniques led to a dramatic increase in the amount of goods for sale. Customers had a much wider choice, and the traditional seller's market turned into a buyer's market.

Companies saw that it was no longer enough just to turn out a good product. They also had to find potential customers and convince them to buy that product. Therefore, they began to put much more emphasis on their sales and advertising efforts.

Marketing went through another

Illustrations by Jon McIntosh

significant change following World War II. At that time production of consumer goods skyrocketed, and many new products were introduced. Companies soon realized that even the most aggressive sales and advertising campaigns couldn't guarantee a product's success if there just weren't enough people interested in buying it.

Some innovative marketers began making extensive surveys to find out what kind of products the public wanted. Using that information, companies developed products precisely targeted to their potential customers. This switch from product-orientation to consumer-orientation marks the beginning of the era of modern marketing.

"The difference between marketing and sales," says Collins, "is that marketing is bringing a product to a customer, whereas sales is bringing a customer to a product. Marketing is before the fact. In marketing we go out and talk to customers and find out what their needs are, then try to create products that will fit those needs."

Like Schweber, Collins is an engineer. He received his BSEE from the University of Tulsa (Tulsa, OK) and his MSEE from Rice University (Houston, TX). Later he earned an MBA at the University of Texas (Austin). Collins worked for two petrochemical instrument companies in Texas designing microprocessor instrumentation for metering natural gas. Many of his colleagues in Motorola's marketing department are also engineers.

Collins feels his engineering background has been invaluable in his present job for two reasons. "One is that engineering teaches you discipline, organization, and an approach to problem solving," he says. "The other is that I understand the technical aspects of the products I'm marketing."

Just as it's important for marketers to understand the engineering that goes into their companies' products, it's equally important for engineers to understand how those products are marketed. Another significant reason why engineers should understand marketing is that it will give them more control over their work.

"Engineers need to have more control over what they're doing," says Holly Stump, director of marketing for Logic Modeling Systems in Milpitas, CA. "In order to get that control they need to understand marketing functions, such as new-project specifications and definitions and the market research that leads to the development of a

project."

Stump holds a BSEE from the Illinois Institute of Technology (Chicago) and an MS in Engineering Management from Stanford University (Stanford, CA). She worked for Hewlett-Packard, first as an IC designer, then as a project manager in an IC design group.

"Part of my charter as an engineering manager was to obtain new business for the designers in my group, so that gave me a little taste of marketing," she says. "The marketing function had a lot of overlap with engineering management, and some of the decisions that are made in marketing can have a much greater impact than even engineering-management decisions can have."

Before a company attempts to introduce a new product, its marketing department devises a strategy and draws up a plan. A marketing plan begins with a target market, the group of potential customers a company wants to reach. Markets can be defined in different ways—by geographical location, by income level, by age, by gender, or by combinations of these and other factors.

Once a target market has been selected, the marketers try to estimate how large a demand exists for the new product. Although there are many techniques for estimating demand, none of them is foolproof. Survey data can be incomplete. Interview subjects can be unreliable. The results of previous marketing efforts can be inapplicable.

Any comprehensive marketing plan has to take into account what some textbooks refer to as the four Ps. A company must develop the right *product*, support it with the right *promotion*, give it the right *price*, and put it in the right *place*.

"In planning the introduction of a new product, the most important thing you have to understand is how that product is going to help the people who are going to purchase it," says Stump. "Without that understanding, you're just going through the motions. You won't be emphasizing the right characteristics of the product. That's one of the reasons having an engineering background is so important."

Engineers also have to understand the long leadtimes involved in marketing. "If an engineer is developing a product and, after a year of work, when it's done, says, 'Here it is—now go sell it,' it's too late," says Schweber.

"Marketing leadtimes are on the order of months and months," he adds. "You have to start on the data sheets and support literature, start on training the sales force, start on your plans for how to promote the product, long before the product is ready, in parallel with the product's design cycle."

Marketing plans involve dozens, sometimes hundreds, of variables. When marketers talk about "place," for example, they don't just mean where customers can purchase products, but also the means used to get products to customers. "Place" can include channels of distribution, transportation, warehousing, inventory control, and retail outlets. Marketers have to organize all of these to make sure that products get to customers at the right time and in the right quantity.

When a product is introduced successfully, the personal satisfaction can be great. "The main satisfaction in engineering is creating a complete and working product and shipping it," says Schweber. "In marketing the satisfaction comes from solving people's problems that weren't solved adequately before. The greatest satisfaction is when the product you have becomes number one in the market, because that means it met people's needs."

Marketing has other rewards as well. "I like getting out and meeting people. I like seeing various applications of products. And I like rolling up my sleeves and helping people design their projects," Collins says.

"In engineering you're a rather independent contributor," says Stump. "In marketing many others are helping you to be successful, and you're helping them. You get a lot of gratification out of being a focal point for many types of activities, such as solving problems and managing outside resources."

Getting started in marketing

The careers of Schweber, Collins, and Stump show that marketing can be a richly rewarding field for an engineer. Moving into marketing can be a logical step for an engineer who wants to get away from the bench and have more interaction with customers. But how can you get started?

"That should be very easy in most companies," says Stump. "What you do is volunteer for more work. Ask the marketing manager or the director of marketing about participating in a marketing program. Everyone in marketing would love to have an engineer volunteer to attend a trade show or give a technical paper or write a technical article for a journal. Marketing people would be delighted to have an engineer be a spokesperson at a product introduction and talk about the product and its utility."

Collins notes that engineers sometimes have a unique opportunity to give themselves some firsthand marketing experience. "Many times after an engineer has designed a new product, until the manuals are written and the sales

force is trained on it, he's the one person in the world who understands that product best. That's his opportunity to spread his wings.

"He could put together a presentation and go out and give it to customers. He could talk to customers and get direct feedback from them. Until information about the product is widely disseminated, he is the point man."

If you don't want to leap right into the front lines of marketing, there are other ways to learn about it. You can write or phone the American Marketing Association, (Chicago, IL), which has 98 chapters across the country, plus 386 collegiate chapters. They will send you an information packet about marketing and put you in touch with your local chapter. The Association sponsors seminars, classes, and luncheons where you can meet professional marketers. They also publish a biweekly newspaper and provide placement services.

Many large companies offer their own introductory marketing courses. Courses are also available in the evening divisions of many colleges and adult-education centers. In addition, working in some areas of engineering, such as applications and field service, will give you direct contact with customers and involve you in some marketing functions. Even if you have no intention of moving into marketing, a solid knowledge of how it affects what you do will help you in your work and show you new options for your career. EDN

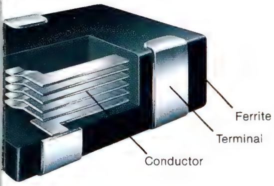
Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

TDK's Total SMT Separates Science Fiction From Science Fact.
Hey, you're looking pretty glum... What's the matter?
SMT Man! You've come just in the nick of time! I need your help! I'm stuck on designing this circuit board.
TDK®

s Total Systems Approach To SMT, Gives

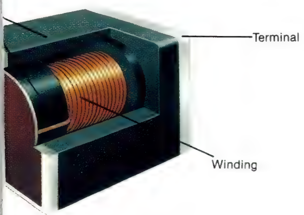
ıip Transformer

ıip transformer has absolutely no
o TDK advancements in magnetic
:ive materials, and multilayer
ransformer features a completely
with inherent magnetic shielding.



ıductor (Wound Micro Chip Inductor)

' was developed to combine
h high inductance up to 1000μH.
sed magnetic circuit structure
tic shielding, making this chip
y mounting applications. It features
and achieves a high Q factor.



MI Filter

EMI Filter, ACF Series, is a
te chip bead and multilayer ceramic
ch has an attenuation of over
650MHz frequency range and
construction accounts for its
shielding characteristics.
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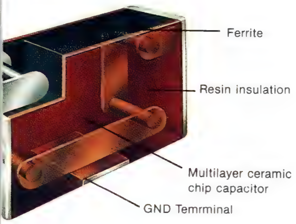
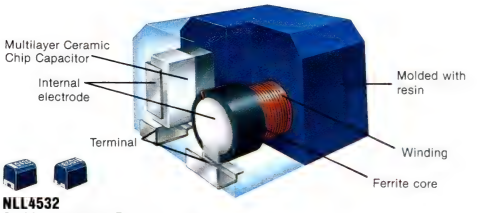
y 1.8mm (.07 inch) thick, it
ch for



Leadless EMI Filter (Wound Chip EMI Filter)

The rendering of the EMI filter into a chip format has been considered essential for the creation of the smallest and lightest electronic products. TDK was one of the first to do it. Our leadless EMI filter is effective against EMI in signal lines, and has been designed for good solderability, thermal resistance, moisture resistance, and mechanical strength.

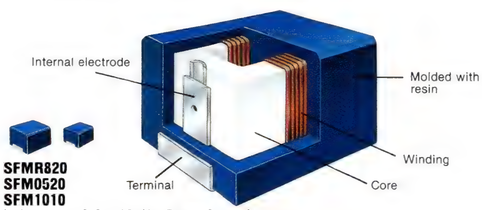


NLL4532
C: 33 ~ 100,000pF L: 1 ~ 220μH

Leadless Line Choke SF Coil

(Wound Chip Line Choke)

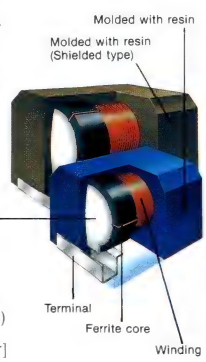
By employing advanced winding technology, TDK has developed magnetic material with excellent absorption of thyristor switching noise. Molded in resin, they are ideal for eliminating EMI in power supply lines for digital circuits.



SFMR820
SFM0520
SFM1010
Inductance: 0.8 ~ 10μH Rated Current: 1-2A

Leadless Inductor/Power-Line Leadless Inductor (Wound Chip Inductor)

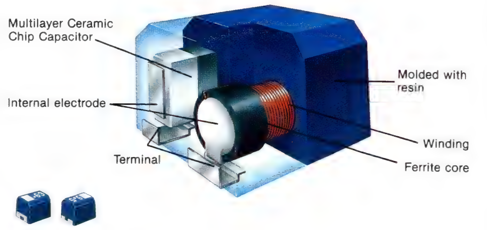
TDK's advanced winding technology together with compact ferrite cores with highly precise performance characteristics are what make TDK Leadless Inductor unique. Power-Line Leadless Inductor is ideal for EMI suppression in power lines with 60 ~ 1800mA current rating. Both feature metal terminals and come molded in resin for maximum reliability.



NL322522 L: 0.01 (450) ~ 220μH (50mA)
NL453232 L: 1.0 (450) ~ 1,000μH (30mA)
NL565050 L: 1,200 (75) ~ 10,000μH (25mA)
NLF453232 L: 1.0 (150) ~ 1,000μH (15mA)
[Shielded Inductor]
NLC322522 L: 1.0 (850) ~ 330μH (60mA)
NLC453232 L: 1.0 (1050) ~ 220μH (120mA)
NLC565050 L: 1.0 (1,800) ~ 1,000μH (85mA)

Leadless LC Trap (Wound Chip LC Trap)

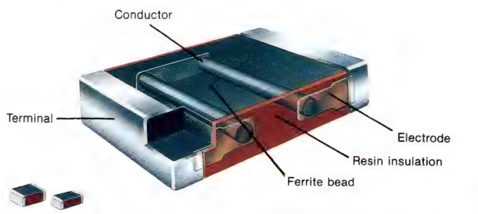
TDK's LC trap is a composite consisting of a miniature coil and a multilayer ceramic chip capacitor. A new proprietary structural design affords highly accurate dimensional control, making this chip well suited for fully automated mounting systems. Metal terminals insure excellent solderability.



NLT4532
F range: 630kHz ~ 13MHz
Tolerance: ±2% Attenuation: 20dB min.

Ferrite Chip EMI Suppressor

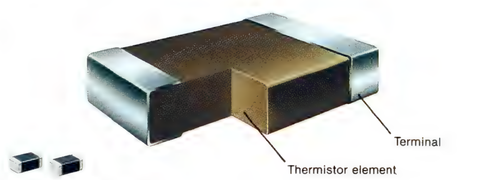
This chip EMI suppressor features proprietary new materials and incorporates the latest advances in chip technology. The device effectively eliminates EMI and prevents parasitic oscillation. A TDK proprietary structural design insures high impedance per volume, and coverage over a wide frequency range.



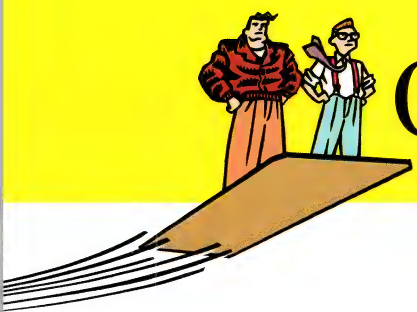
ACB201209 Zo: 7, 10, 11Ω
ACB321611 Zo: 19, 26, 31Ω
ACB322513 Zo: 31, 52, 60Ω
ACB453215 Zo: 70, 120, 125Ω

NTC Chip Thermistor

The Negative Temperature Coefficient chip thermistor is a temperature compensation device. Although in chip form, it has the same basic performance characteristics as conventional lead-type NTC thermistors. The NTC chip thermistor can also be utilized to make a temperature compensation circuit on a PC board. Nominal resistance and temperature characteristic tolerances have been reduced to extremely low levels.



NTC CS3216 R typical:
1.0 ~ 150kΩ at 25°C
Temp. Range: −25 ~ +85°C

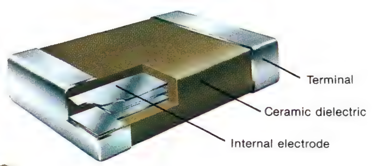


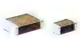
Complete Integration, TDK's

Simplifying High Density Placement-TDK Surface Mount Devices

Multilayer Ceramic Chip Capacitor

This line of capacitors offers a wide range of capacitances, temperature characteristics, and sizes, with terminals designed for excellent solderability. As a leading manufacturer of ceramic capacitors, TDK remains committed to bringing you the highest possible product reliability and stability at all times.

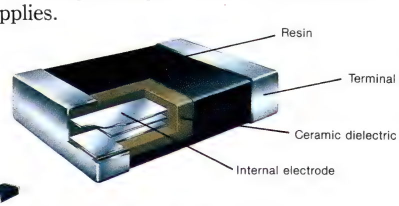


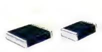


C1608 (CC0603) C: 0.5 ~ 220,000pF
C2012 (CC0805) C: 0.5pF ~ 1μF
C3216 (CC1206) C: 0.5pF ~ 2.2μF
C3225 (CC1210) C: 750pF ~ 3.3μF
C4532 (CC1812) C: 2,400pF ~ 1μF
C5650 (CC2220) C: 5,100pF ~ 1.5μF

Large-Capacitance Multilayer Ceramic Chip Capacitor

Large-capacitance multilayer ceramic chip capacitor covers the capacitance range normally associated with electrolytics. It features a non-polarized construction and a long life. This large-value capacitor is seeing widespread use in switch-mode power supplies.

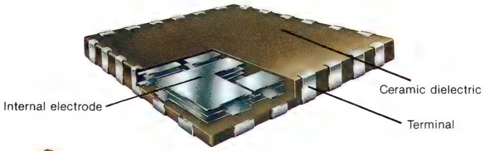


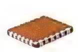


HC8050 C: 1.5 ~ 6.8μF
HC1063 C: 2.2 ~ 10μF
TC: +20, −30% (−25 ~ +85°C)
HC1280 C: 3.3 ~ 22μF
HC1612 C: 10 ~ 47μF

Multilayer Ceramic Chip Capacitor Network

Through advanced multilayer and integration processes, TDK can incorporate a network of 12 ceramic capacitors into a single chip, with your choice of capacitances and interconnection topologies. In addition, these networks are made of high-performance insulating materials, allowing other chips to be mounted directly onto the surface. This provides compatibility with the new generation of hybrid chip designs.

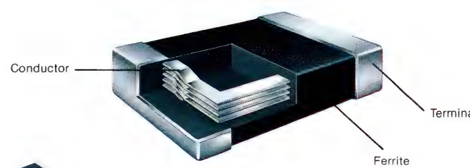


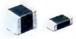


MCN7575
TC; COH, 1 ~ 100pF (12 capacitors)
; SL, 10 ~ 1,000pF (TC: −1,000 ~ +350ppm/°C)
Class II, 100 ~ 470,000pF (12 capacitors)

Multilayer Chip Inductor

TDK created the world's first inductor without windings by using alternating layers of ferrite paste and conductive silver paste. The unique properties of TDK ferrite give a monolithic closed magnetic circuit with excellent shielding properties, for suitability in high-density configurations. A whole series of multilayer chip inductors are available, starting with the smallest 2012 series. They measure only 2.0 × 1.25 × 0.6 to 1.25mm (.079 × .049 × .024 to .049 inches).

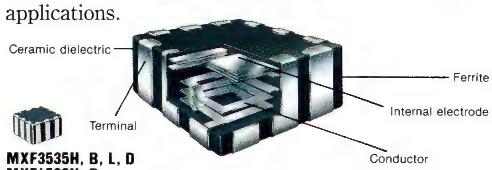




MLF2012 L: 0.047 ~ 33μH
MLF3216 L: 0.047 ~ 33μH
MLF3225 L: 39 ~ 220μH

Multilayer Chip LC Filter

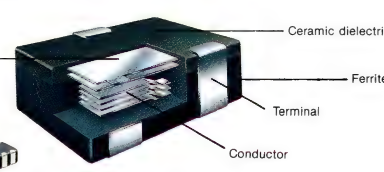
TDK's multilayer technology and simultaneous sintering of magnetic materials and ceramic dielectric materials have created this advanced chip LC filter. An inductor, transformer, and capacitor are layered and integrated into a single monolithic chip measuring only 5 × 5 × 2.8mm (.197 × .197 × .110 inches). This closed magnetic circuit eliminates cross talk and makes this chip ideal for high-density mounting applications.

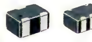


MXF3535H, B, L, D
MXF4532H, B
MXF5050H, B, L, D
HPF, BPF, LPF, Delay Line

Multilayer Chip LC Trap
Multilayer Chip IF Transformer

This Multilayer Chip LC Trap and Multilayer Chip IFT feature new chip construction obtained by the simultaneous sintering of different materials, such as ferrite and conductive and ceramic dielectric. Both house closed monolithic magnetic circuits which eliminate cross talk. Their compact size is ideal for high density mounting.

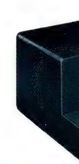


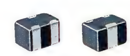


MXT4532
MXT5050
F: $f_0 \pm 3\%$
F range: 700kHz ~ 10MHz
MIA4532 F: 455kHz
MIF4532 F: 10.7MHz

Multilayer Ch

This innovative ch
windings, thanks t
materials, conduct
technology. The t
monolithic design,

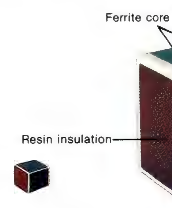




MTT4532 L: 10 ~ 200μH

Micro Chip In

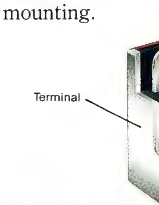
This chip inductor
miniature size wit
Its proprietary clo
insures full magne
ideal for high-densi
low DC resistance



ACL3225S
L: 0.01 ~ 1,000μH

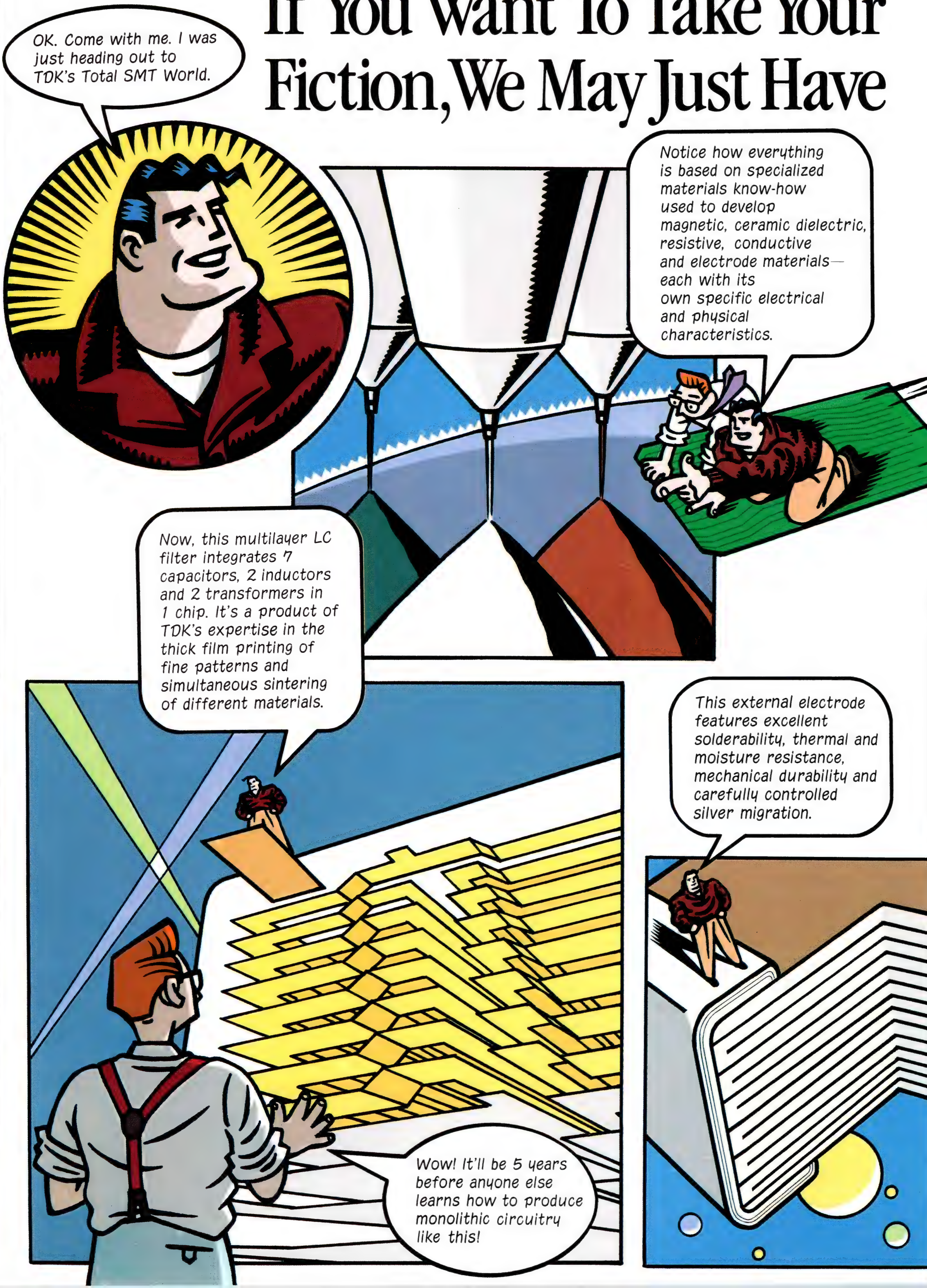
Micro Chip F

This Micro Chip
combination of ferr
chip capacitor. Ea
25dB in the 4.5 to
its compact ferrite
excellent magneti
In addition, becau
ACF Series, is on
matches IC pin pi
high density
mounting.

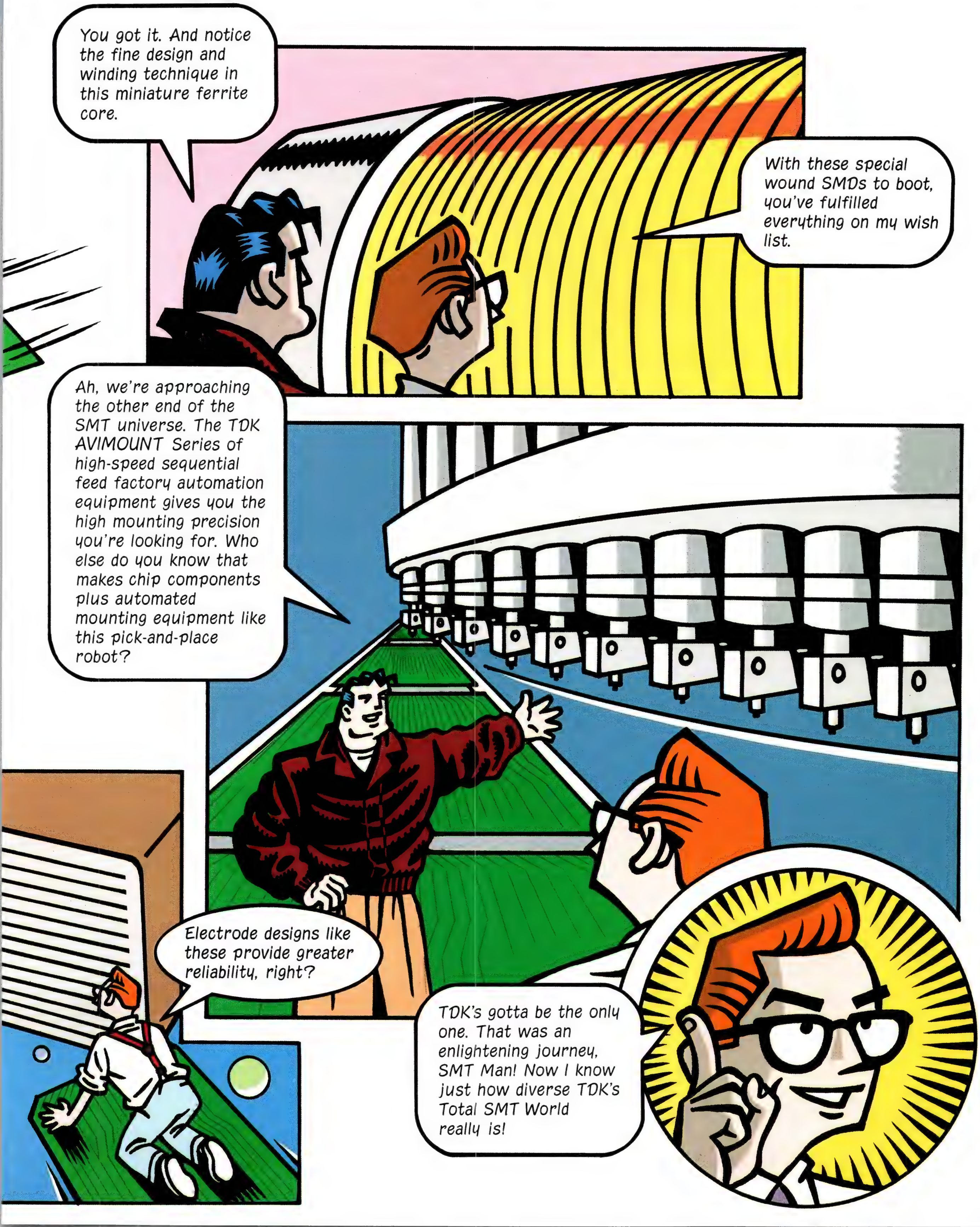


ACF453218
Attenuation: 25dB min.
F range: 4.5 ~ 650MHz

If You Want To Take Your Fiction, We May Just Have



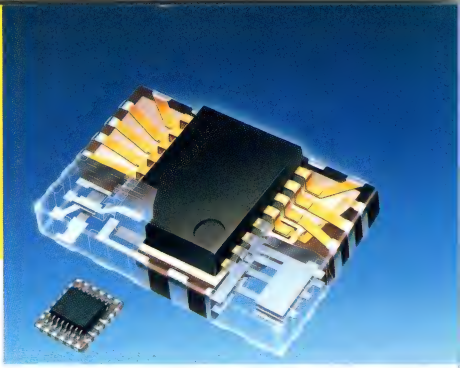
Applications Out Of The Realm Of The Approach To SMT You Need.



ty Edge.

Multilayer Hybrid Circuit

TDK Multilayer Hybrid Circuit, used as an equalizer amplifier, integrates 16 capacitors, 16 resistors and 1 IC all on a single chip and measures 8.5×7.0×2.4mm (0.33×0.28×0.09 inches).



y Line is of a
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of original TDK
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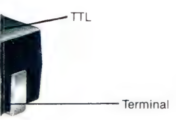
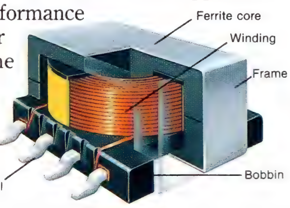
chip capacitor.
able compact unit.



tilayer ceramic chip capacitor

SM Transformer/Inductor

TDK's highly miniaturized transformer/inductor is designed for today's high-density surface mount applications. The component features two distinct cores: one high-permeability ferrite core, and one low-loss ferrite core with high saturation magnetic flux density. The former is well-suited for applications requiring a high-performance pulse transformer or wide-band transforme while the latter is optimized for high-performance DC to DC converters.

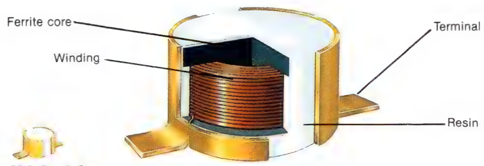


EE5, EE12, ER9.5, ER11/5, ER14.5/6, T2

SM Step-up Inductor

(For Unimorph Piezoelectric Buzzer)

This miniature step-up inductor features high inductance, and works with the unimorph piezo-electric buzzer circuit to produce high sound pressure levels. The inductor is compatible with fully automatic mounting systems.

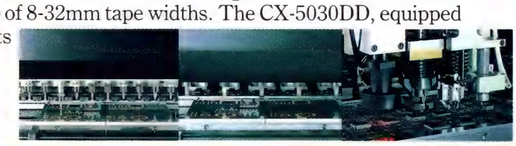


OL3.3×1.6
OL3.3×2.1

nt CX-5A CX-5230NS CX-5030F / CX-5 CX-5030DD CX-5030DV

Automatic Chip Component Mounter

ideal for upgrading line capability according to the
exible, the CX-5230NS has 10 nozzles to mount 8-32mm
30F has five nozzles to mount odd shaped components.
5030DV have two mounting heads. These machines
.) of 8-32mm tape widths. The CX-5030DD, equipped
nts
V,



Mountable component types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
30 types	0.65 sec.	Max. 457L×356W (17.99L×14.02W) Min. 90L×60W (3.54L×2.36W)	1180L×1160W×1573H (46.46L×45.67W×61.93H)
15 types	1.1 sec.		
30 types	1.2 sec.		
30 types	3.3 sec.		

nt CX-6 CX-6160

Automatic Chip Component Mounter

, two mounting
AVIMOUNT CX-6
) components/hr.
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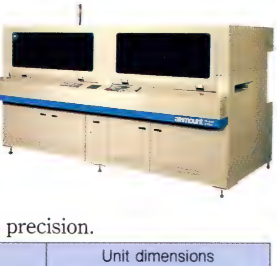
shed by simple
manufacturing of
onent changeover.
e system
s components, thereby assuring high mounting precision.



able nt types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
pes	0.3 sec.	Max. 457L×356W (17.99L×14.02W) Min. 90L×60W (3.54L×2.36W)	2980L×1430W×1548H (117.32L×56.30W×60.94H)

AVIC-7800EX

Satellite Computer System

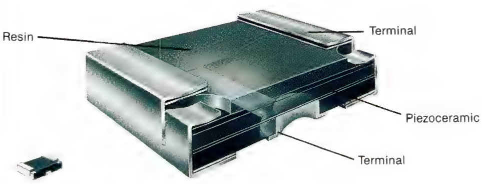
The AVIC-7800EX satellite computer system can control up to eight AVIMOUNT machines. When you put an AVIC-7800EX in your production line, you get equal load capacities since program instructions are dispensed in a well-balanced manner.

FUNCTIONS
1) DNC communications 2) Achievement and schedule management 3) Sequential manufacturing line management 4) Machine control 5) NC Program management 6) Automatic program generation for respective machines 7) Program compiling and editing for respective machines 8) Communication with the host computer in TDK standard format.

You A Powerful Design And Productivi

Ceramic Chip Filter • 10.7MHz

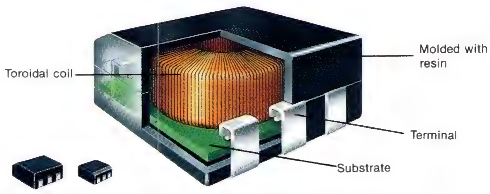
Compact TDK 10.7MHz Ceramic Chip Filter for FM tuners is perfect for automatic mounting (6.4×3.3×1.2mm—.25×.13×.05 inch). Its original capsulated metal terminals allow for excellent solderability and prevent silver migration.



CEF1070
F: 10.7±0.03～±0.12MHz

SM Pulse Transformer

This surface mount pulse transformer achieves miniaturization through advanced winding technology and a small, high performance toroidal ferrite core. Its high level of reliability makes it ideal for signal transmission applications.

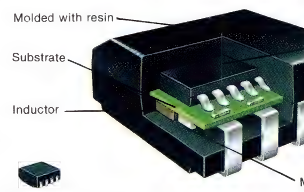


CPT6×6 L: 10～100μH
Winding ratio N1:N2; 1:1

CPT10×10 L: 100～1,000μH
Winding ratio N1:N2:N3; 1:1:1

SM Active Delay Line

This Surface Mount Active Dela
5 output lumped constant nature
Fast TTL elements. A product
design, each active delay line is
inductor and multilayer ceramic
Together they form a highly reli



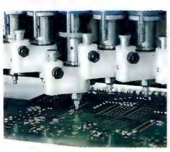
SAD Delay Time: 20～250nsec.

Systematization - TDK Automated Mounting Technology

avimount RX-4A

RX-4260
Automatic Chip Component Mounter

The AVIMOUNT RX-4260 high-speed mounting system is ideally suited to factory automation requirements. It features a rotary disk head—an industry first. In addition, the RX-4260 has a sequential supply system for easy batch changeover and for communication with the system's host computer. And, since the RX-4260 is a core machine, it can link with other types of machines for increased component mounting capacity. For example, an RX-4260 linked to a CX-5030 mounter can handle up to 90 different types of components.

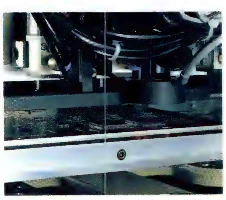


Model	Component supply	Mountable component types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
RX-4260	8, 12mm taping	60 types	0.29 sec.	Max. 381L×305W (15.00L×12.01W) Min. 150L×100W (5.91L×3.94W)	2460L×2200W×1600H (96.85L×86.61W×62.99H)

avimount CX-4A

CX-4240
IC Mounter with Vision Cameras

The AVIMOUNT CX-4240 is a special-purpose mounting system designed for extremely high mounting precision. A system with two high-resolution vision cameras detects and corrects skewed positions, bent leads and planerity, and fiducial marks on the PC boards. Any problems are quickly corrected, for high levels of precision and accuracy. The CX-4240 handles flat package ICs, and can accommodate up to 40 types of SOPs, QFPs, PLCCs, and LCCs. The 3-nozzle design enables the mounting of three ICs in a single operation, with speeds as fast as 2.5 seconds per component.



Model	Component supply	Mountable component types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
CX-4240	12～36mm taping, TAPE PAK®, MSPAKs	40 types	2.5 sec.	Max. 508L×457W (20.00L×17.99W) Min. 90L×60W (3.54L×2.36W)	1800L×1410W×1590H (70.87L×55.51W×62.60H)

avimou

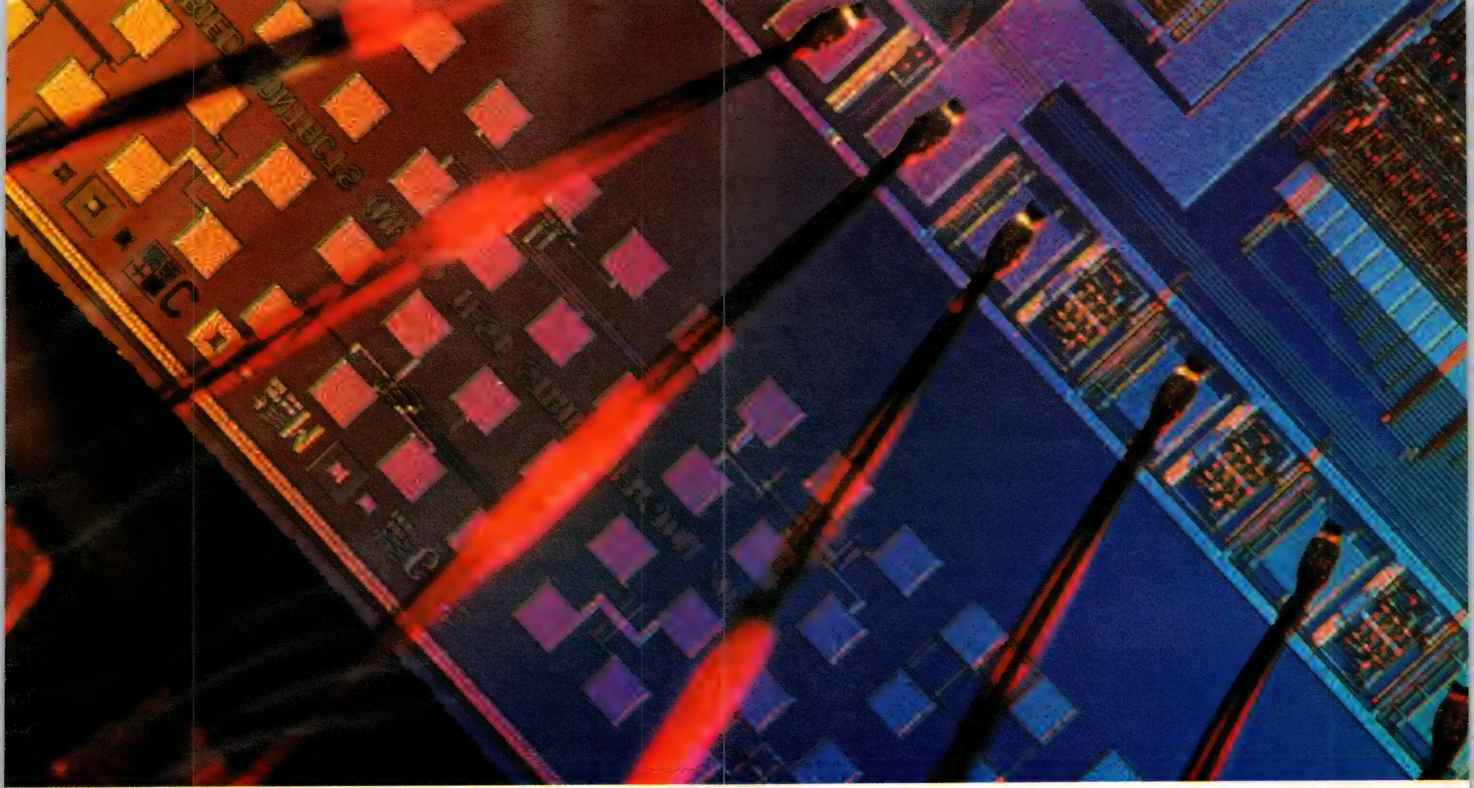
The AVIMOUNT CX-5 Series is
manufacturing scale. Compact and
taping components and the CX-5
Both the CX-5030DD and the CX
mount 30 types of components (ma
with a dispenser, mounts compon
onto solder paste. The CX-5030I
equipped with vision cameras,
precisely mounts components by
utilizing image processing.

Model	Component supply
CX-5230NS	8～32mm taping
CX-5030F	16～32mm taping, stick
CX-5030DD	8～32mm taping
CX-5030DV	8～32mm taping, stick, tray

avimou

A complete FMS package in its
heads and one sequence head let th
realize a mounting speed of 12,(
Each mounting head has 20 noz
can handle a maximum of 160 ty
from micro chips to odd shaped
Lot changeover is easily accomp
programming, allowing continuc
various types of PCBs without co
Equipped with a vision camera,
automatically centers and positi

Model	Component supply	Mo compo
CX-6160	8～32mm taping, stick	160



MAKING CONCEPTS REALITY

Rockwell Graphic Systems is the leader in the development of the most technologically advanced newspaper and commercial printing equipment in the world. As a division of **Rockwell International**, a multi-national Fortune 100 Corporation, we're dedicated to developing new products and technologies to increase productivity and production quality for our domestic and international customer base of newspaper publishers and commercial printers.

Our software engineering professionals help us realize our unequaled performance and innovative technologies which extend beyond state-of-the-art. Their expertise, persistence, initiative and dedication has brought us to the forefront of leading technologies.

To promote our leading position and to continue to meet our future goals, we're seeking talented and experienced software engineering professionals who possess the commitment necessary to make concepts reality.

Software engineering opportunities currently exist at the following levels:

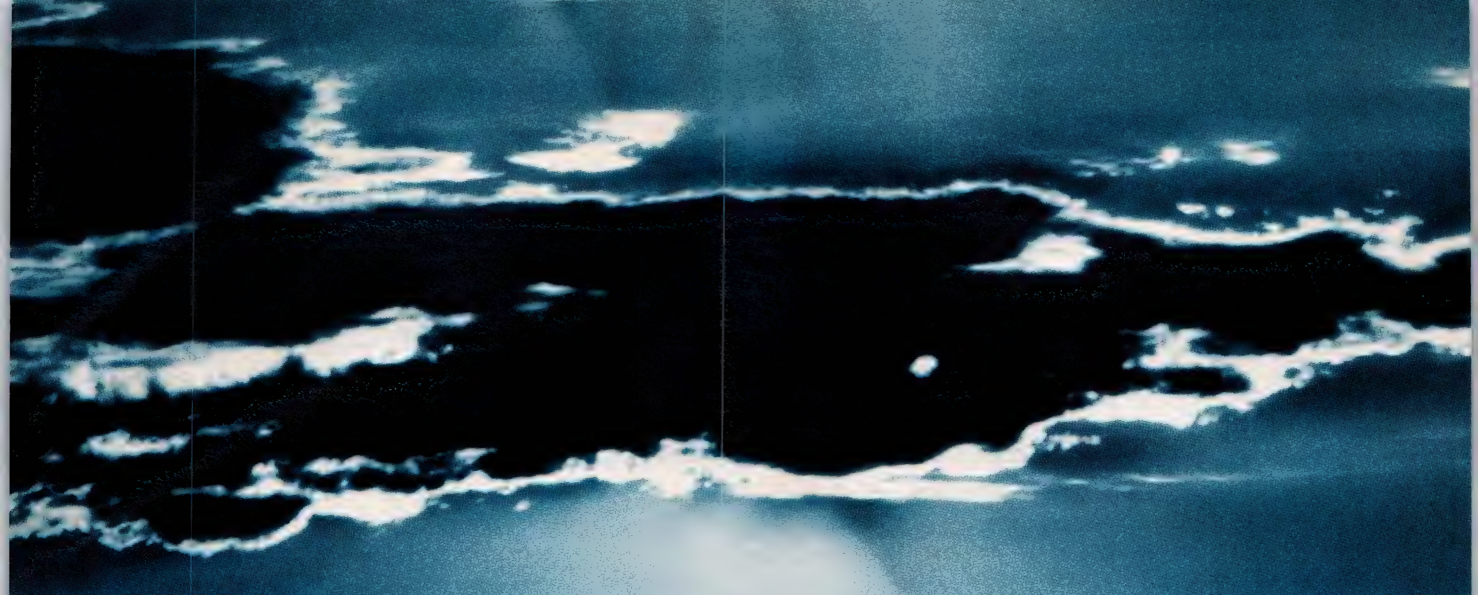
- **STAFF ENGINEER**
- **PRINCIPAL ENGINEER**
- **SENIOR ENGINEER**
- **DEVELOPMENT ENGINEER**

Selected candidates will possess a B.S. or M.S., or working equivalent, in software engineering or similar discipline and appropriate related experience.

Rockwell Graphic Systems offers a highly competitive salary and benefits package which includes life/medical/dental insurance, tuition reimbursement, a 401(K) savings plan and a pension plan. To learn more about these opportunities, please send your resume complete with salary history to: Staffing Manager, Dept. C190, **Rockwell Graphic Systems Division**, 700 Oakmont Lane, Westmont, IL 60559. Equal Opportunity Employer M/F/H/V.

Rockwell International

...where science gets down to business



HONEYWELL AND YOU: A WINNING COMBINATION FOR THE 90s AND BEYOND.

Honeywell in Phoenix offers a variety of career opportunities in our Commercial Flight Systems Group. Our continuing growth has created the following positions:

Systems Design Engineer — In this area, you will be involved in guidance and control systems analysis and hardware/software design trade-offs. Specification designs, including guidance, navigation and control algorithm development, as well as systems integration and installation, flight test and customer liaison activity, are a part of these positions.

System Software Development — This area involves development of flight software for advanced guidance and control systems for aircraft using modular and structured programming techniques. You will be involved with algorithms and development of real-time programs in both assembly (8086 family Z8002, 68000) and high order languages such as Pascal, "C," Ada and PLM/86, with subsequent hardware integration.

Electronics Engineering — These positions involve the development of new processor/bus architectures and specifications to support fault tolerant/redundant airborne applications. To qualify, you should have experience with embedded multiprocessor-based avionics systems.

Display Systems — These positions offer systems, software and hardware opportunities with CRT/LCD display technology. You should be familiar with digital hardware design and/or real-time programming. Systems functions include overall system definition, design and customer interaction.

To qualify for the positions listed above, you should have a BSEE or a BSCS degree and at least three years of experience.

Manufacturing Engineering — These positions offer support of new product transitions to production, on-going operations sheet and tooling requirements and implementation of floor work teams. You will interface with a number of functional areas and assist in the implementation of shop floor control, SPC and JIT systems. To qualify, you should have an engineering degree in mechanical, manufacturing, industrial or a related engineering discipline, with two or more years of experience in manufacturing engineering or a related product engineering role supporting electromechanical or circuit card assembly. Experience in surface-mount technology, SPC and/or JIT implementation is a plus.

Quality Engineering — To qualify for this position, you should have a BS degree in an engineering curriculum. A minimum of two to five years of experience in quality engineering/assurance, reliability and/or product engineering is required. You should have strong communications skills and computer applications experience. Customer interface experience is preferred.

Additional opportunities are available in:

- CRT/LCD Display Technology
- Avionics Systems Simulation
- CAE Engineering (Apollo Mentor Systems)
- Artificial Intelligence
- VAX Systems Administration
- Fiber Optic Pressure Sensors
- EMI/HERF
- Software Tools Development

Make a career move. Honeywell offers you a competitive salary and benefits package and the opportunity to live in the year-round outdoor lifestyle of Phoenix. All new employees are required to successfully complete a drug screening test. Send your resume and salary history, in confidence, to Honeywell, Commercial Flight Systems Group, Professional Employment (EDN-E844), P.O. Box 21111, M/S I-17C, Phoenix, AZ 85036.

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U.S. citizenship required for some positions

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Stretching from the U.S. throughout the Far East, Latin America and Europe, Motorola cell sites cover the world. In fact, the company that pioneered cellular communications is now outdistancing all competitors combined. We're bringing the worldwide telecommunity closer and paving the way for even greater breakthroughs...like our patented four-cell reuse plan that supports more voice channels with fewer cell sites.

And with just 1% of the global cellular market developed, the opportunities at Motorola Cellular have just begun. We're developing the most advanced software, switching equipment and radio telephone exchanges. We're constantly modifying, updating and simplifying systems while enhancing RF sector-sharing capabilities.

Flexibility, capability and expandability...that's what Motorola Cellular can offer its customers...and your engineering career. If you want a career as dynamic as our growth, set your sites on one of the opportunities on the opposite page.

We offer an attractive salary, a comprehensive benefits package and opportunities for professional growth. For immediate consideration, please send your resume to: Supervisor, Professional Recruitment, Motorola Inc., Cellular, 1501 West Shure Drive, Arlington Heights, IL 60004. Or FAX your resume to: (708) 632-5717 (our 24-hour FAX line). To access our On-Line Career Network from your PC, dial (508) 263-3857, press return twice, and key in password LEGACY. We are an equal opportunity/affirmative action employer.

MOTOROLA

Cellular Subscriber Group

Radio Telephone Systems Group

1990
1991
1992
1993
1994

SOFTWARE: Real-time software development using C, UNIX*, Pascal, Ada, assembler and structured design; experience in software quality, metrics, or testing; CASE software tools (Sun, Apollo); design, programming and system debugging for telephone digital switching or data communication systems; assembler and high-level structured languages; hardware diagnostics; object oriented design, C++; software development tools such as Teamwork and Interleaf; ASN.1 (Abstract Syntax Notation); data communications protocols (CCITT #7, OSI, X.25, X.75, PAD, LAPB, LAPD, Ethernet, ISDN, CCITT V series modem, group 3 fax); modeling and simulations (GPSS, SIMSCRIPT and other simulation tools). BSEE/BSCS/BSCE or equivalent. Respond to Dept. SW.

ELECTRICAL/COMPUTER: Analog and RF circuit design, receiver or transmitter RF circuits; LCD display technology, acoustics, and 8-bit microprocessor software; infrared and fiber optics; low speed data; digital modulation; 900 Mhz RF power amplifier design with hybrid or microstrip circuitry; RF device development with device vendors; parallel and/or push-pull RF amplifier design at 900 Mhz or UHF; A/D and D/A convertors; RF propagation; passive and active filter theory; microwave antenna design; UL, EMI and RFI requirements; HP 3062 test system; HP 9000; digital hardware, microprocessor applications and interfaces; digital switching technology; firmware development methodology; PCM and digital telephony; digital signal processing; ASIC design; LAN systems, PSTN standards, ISDN standards, processor architectures, high-speed logic; 16-bit MPU design practices, programmable logic; digital modulation synchronization, adaptive signal processing, viterbi algorithm and MLSE, decision Feedback equalizer; convolutional code and linear block code, speech coding, echo cancellation, encryption; CAE techniques for digital hardware design using Mentor Graphics, etc.; data communications protocols (CCITT #7, OSI, X.25, X.75, PAD, LAPB, LAPD, Ethernet, ISDN, CCITT V series modem, group 3 fax); computer network management/administration (Apollo, Sun, Mentor Graphics, AppleTalk). BSEE/MSEE/ BSCE/BSCS or equivalent. Respond to Dept. EC.

MECHANICAL: Electronic packaging; CAD, CV CADDS 4X; materials selection and geometric tolerances and dimensioning; extruded metal; injection molded plastics; life test procedures and factory introduction and support; plating materials and processes; structural analysis modeling; die casting and sheet metal stampings; thermal management. BSME/ MSME or equivalent. Respond to Dept. ME.

SYSTEMS: Radio/cellular communication systems engineering; RF propagation prediction methods; PSTN traffic planning; telephone network, interconnection and telecommunication industry standards; microwave system design and equipment engineering; telephone switching systems; software programming skills. BSEE/BSCE/ BSCS or equivalent. Respond to Dept. S.

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Project Engineers: Take projects from "concept to customer." BSME with minimum of 5 years experience with internal combustion engines (gasoline and diesel), mechanical devices, drive trains, and engine management systems.

Design Engineers: CAD experience plus a 2 or 4 year degree in mechanical design with knowledge of materials, stress analysis, manufacturing processes, and layout techniques.

Engineering Technicians: Experience in prototype development model shop practices, mechanical assembly and hand tool use. 2 year Associate Degree helpful. Also need specialists in electronics and electrical products, gears/gear trains. Experience in troubleshooting, testing, and diagnosing items related to internal combustion engines.

We offer competitive salary and benefits, an excellent relocation package and most importantly, an opportunity to be recognized for individual contributions to the industry leader. Submit resume in confidence to: **Mercury Marine, Attn: Dale Wagner, 3003 North Perkins Road, Stillwater, OK 74075-2299.** An Equal Opportunity Employer M/F/H.

MERCURY
MARINE

Employment Opportunity

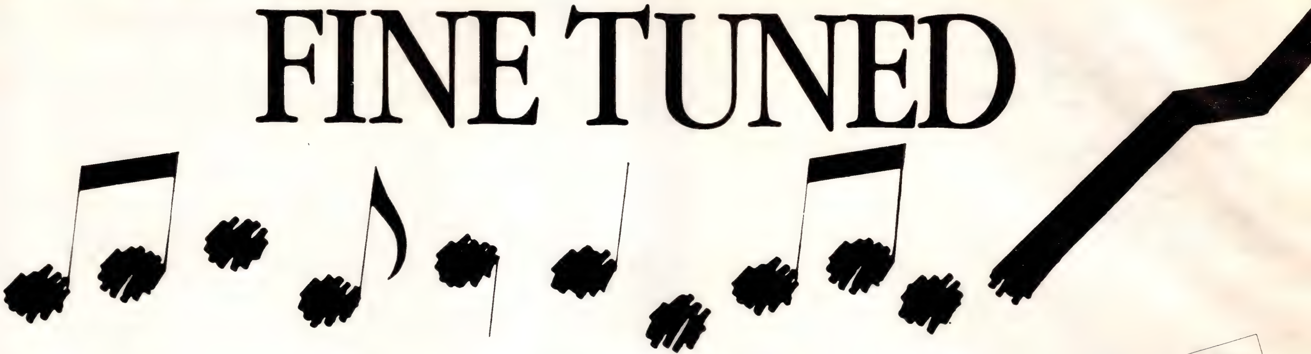
Company needs an applicant who must have B.S. in Mechanical Engineering with at least 2 years experience as software Engineer and must have knowledge to use Computer Languages C and Assembly. Will do research, design and develop high performance graphics controllers for the applications in Computer-Aided Design (CAD), and to implement the drafting software for Mechanical/Electronic Computer-Aided Design and Manufacturer Adaptor. 40 hrs./week, $31,100.00/year. Please submit resume to Mrs. Jimmie Gaston, Div. of Employment Security, 505 Washington, St. Louis, MO 63101, re: Job #354036.

Employment Opportunity

Our company needs an applicant who must have M.S. Degree in Computer Science and knows how to design and implement data base management system, to implement natural/structure language processing, to design and implement a multi-window (screen) online instructional system and to use code generate concept and C and Pascal-2 computer languages. Applicant will design, develop, engineer, manage, test and maintain the software package of "selective ticker"; will manage, direct and analyze the computer programming; and will test the specialized software systems developed. 40-hour week, $35,100/year. Please submit resume to Mrs. Jimmie Gaston, Dir. Employment Security, 505 Washington Street, St. Louis, MO 63101, re: Job #35418.

ORCHESTRATING DESIGN SOLUTIONS

FINE TUNED



Cadence's performance in IC Design Automation is receiving critical acclaim worldwide. As the industry's newest $100 million company, we're bringing audiences to their feet with completely integrated design solutions that have customers up and running in no time flat. Of course, we're not stopping there. We're positioning ourselves to become leaders in the overall Electronic Design Automation (EDA) market.

To achieve this, we have software development teams that cover the entire range of EDA, including IC, CAE, Systems, and Analog. If you're the kind of performer who can win rave reviews, consider Cadence. The critics' choice.

IC R&D

- Software Development Engineers
  - Design Methodology & Solution
  - Data Translation
  - Back Annotation Development
  - Data Translator Design
  - Layout Verification
  - Software Porting
- UNIX* Systems Programmer
- Quality Analyst
- Case Manager

Refer to Job 300-EDNHK/RD

SYSTEMS R&D

- Software Development Engineers
  - Systems R&D Vendor Design
  - Design Entry
  - Design Synthesis Interface
  - Engineering Documentation Tool
  - CAE Library Development
  - Simulation Interface

Refer to Job 350-EDNRD/MF

ANALOG R&D

- Software Development Engineers
  - Mixed Mode Simulation
  - Analog Physical Design
- IC Applications Engineers
- Marketing Manager
- Product QA Engineer
- Analog Specialist
- Technical Writer

Refer to Job 380-EDNHK/MF

CORPORATE MIS

- Telecommunications Manager
- Senior Systems Administrator

Refer to Job 421-EDNHK

DOMESTIC SALES

- IC Applications Engineers
  San Jose, CA   Edison, NJ   Phoenix, AZ
  Denver, CO   Dallas, TX   Orlando, FL
- Sales Representatives
  San Jose, CA   Irvine, CA   Edison, NJ
- Asian Sales Development Engineer
- Domestic Sales Engineer
- Associate Program Manager
- Administrative Assistant

Refer to Job 200-EDNMF/RD/CD

MARKETING

- IC CAD Software Product Marketing Manager
- IC CAD Software Product Marketing Director
- IC CAD Software Product Marketing Engineer
- Director, Hardware Vendor Relations

Refer to Job 110-EDNMF

OPERATIONS

- QA Engineer
- Systems Training Engineer
- Consulting Engineer
- Senior Technical Writers
- Senior Technical Editor
- Systems Administrator

Refer to Job 500-EDNHK

FINANCE/ADMINISTRATION

- Contract Specialist
- Accounts Receivable Staff Accountant
- Treasury Analyst
- Financial Analyst
- Legal Administrative Assistant

Refer to Job 400-EDNCD/JC

CORPORATE APPLICATIONS ENGINEERING

- IC Applications Engineer

Refer to Job 220-EDNJC

JAPAN OPPORTUNITIES

We have the following opportunities available in our facility in Tokyo, Japan. You must speak fluent English/Japanese, with a strong comprehension of the Japanese culture.

- Applications Engineers
- Software R&D Engineers
- Software R&D Managers
- Sales/Marketing Engineers
- Documentation/Translation Specialist

Refer to Job JPN-EDNJC

ADVANCED CAE DIVISON Lowell, MA

The Advanced CAE Division of Cadence is involved in HDL-based design entry and analysis, simulation technology (Verilog®, VHDL) and modeling. We have positions open on all levels for: Software Engineers and Project Leaders in Lowell, MA and San Jose, CA.

Refer to Job ACD-EDNEM

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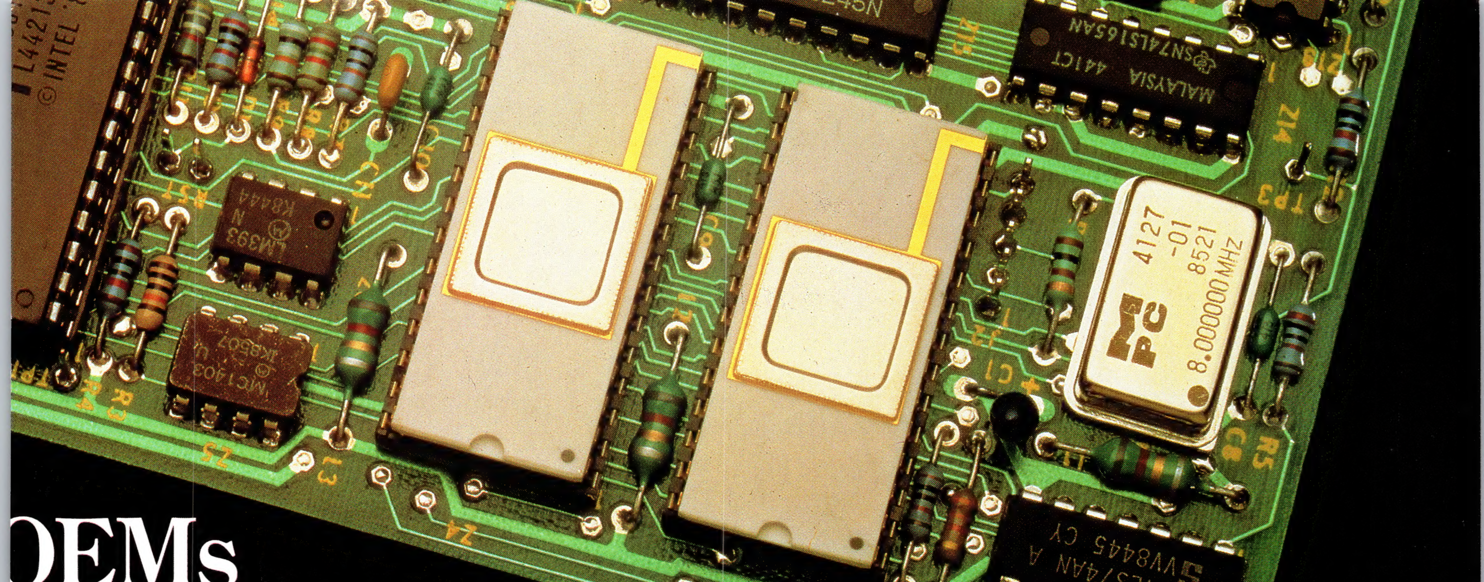
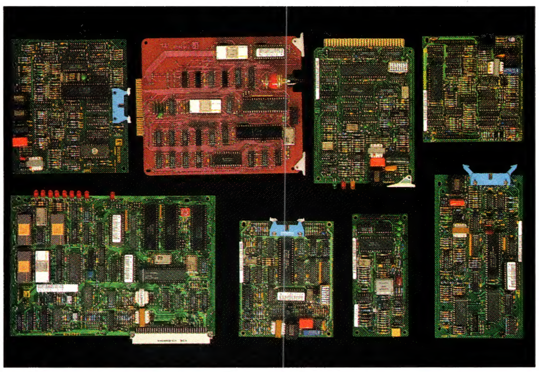


OEMs and modems: four cost effective reasons to have UDS in your corner



1. Concentration: spend your time and money on what you do best.

You excel at what you do; we excel at designing and producing modems. Devote yourself to developing and marketing your products more effectively, and get the modems you need from us. We have invested heavily in automated production equipment, test instrumentation and a large technical staff so you won't have to.

2. Reliability: because nothing costs like something that doesn't work.

Once you receive an OEM modem from UDS, install it, ship it and forget it. Our quality assurance procedure ranges from incoming chip burn-in to 100% testing of all modems prior to shipment. This attention to quality assurance has put our historical reliability rate near the 99th percentile.

3. Experience: we have already solved most of your problems.

Over the past 20 years, we have designed, produced and delivered more than 2 million modems in over 3,000 different configurations. We have proved our capability to fulfill nearly any form, fit and function requirement from 0–300 to 56,000 bps.

4. Commitment: more than a promise, it's our reputation.

Supplying an edge in price/performance begins and ends with commitment. UDS is committed to the manufacture of modems – and only modems. We're also committed to the needs of OEMs, who buy over 30% of the modems we make. We have built a position as an industry leader by honoring commitments – commitments to your quality demands, commitments to your deadlines, commitments to your demand for value.

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Contact us, and we'll help you corner your share of datacomm market. Let's talk specs and prices!
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Telephone: 205/721-8000; FAX: 205/721-8926.

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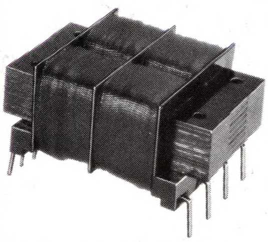
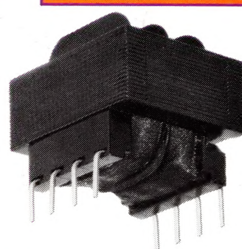
THE FLATHEAD® LP SERIES



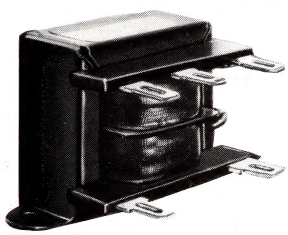
- Low profile for close PC board spacing from a minimum of 0.650" to a maximum of 1.375"
- Dual primary...115/230V, 50/60 Hz
- 5 through 230V outputs; at 10mA through 9.6A; 2.5 VA through 48 VA
- Maximum power in minimum volume

THE SPLIT/TRAN® ST SERIES



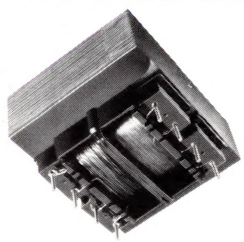
- Smaller footprint for maximum PC board component density
- 50/60 Hz...115V or 115/230V primary
- 5 through 120V outputs; at 10mA through 7.2A; 1.1 VA through 36 VA

THE 2-4-1 SERIES



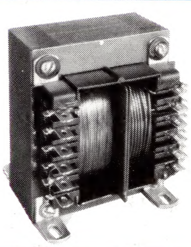
- Chassis mounting
- Solder *and* quick-connect terminals
- 50/60 Hz...115V or 115/230V primary
- 10 through 120V center-tap outputs; at 20mA through 10A; 2.4 VA through 100 VA

THE ONE-4-ALL™ SERIES



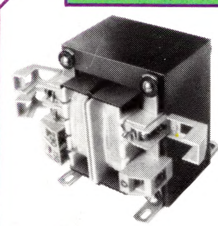
- VDE certified
- UL recognized and CSA certified
- Dual primary...115/230V, 50/60 Hz
- 5 through 36V outputs; at 70mA through 11.2A; 2.5 VA through 56 VA

THE ALL-4-ONE™ SERIES



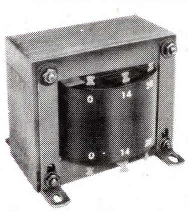
- VDE certified
- UL recognized and CSA certified
- Chassis mount...solder *and* quick-connect terminals
- Dual primary...115/230V, 50/60 Hz
- 5 through 230V outputs; at 110mA through 35A; 25 VA through 175 VA

THE MORE-4-LESS™ SERIES



- High power, isolation/step-down transformer
- VDE certified
- UL (544 & 506) recognized and CSA certified
- Shrouded terminals...screw *and* quick-connect terminals
- Choose between 105/115/125V or 210/230/250V primary
- 115V secondary
- 300, 600, 1000 VA ratings available

RECTIFIER POWER TRANSFORMER LINE



- Signal's rugged high power series
- 115V primary
- 5 through 80V output; 1 through 200A, 10 VA through 2.8 KVA
- Dual center tapped secondaries for maximum flexibility

POWER ISOLATION TRANSFORMER LINE

- Industrial grade stepup/stepdown
- Dual primary; 110/220V, ¼ through 10 KVA
- Available with 110/220V or 220/440V dual secondary
- Taps on primary and secondary allow ± 15% output voltage adjustment

CIRCLE NO. 87